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ELECTROPHOTOGRAPHIC PATTERNING FOR LARGE AREA ELECTRONICS

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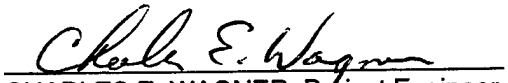

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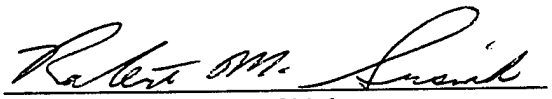

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13. ABSTRACT *(Maximum 200 words)*

The goal of this program was to develop an electrophotographic patterning method for Thin-Film Transistors (TFTs) fabrication. The current Active-Matrix Liquid Crystals Display (AMLCD) fabrication method uses multi-step photolithographic masking, deposition, and etching. The objective of this effort was to explore processing alternatives that would eliminate the use of photolithographic equipment and thereby reduce the cost of fabricating TFTs for AMLCDs.

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I. Project Description

The goal of this program was to develop an electrophotographic patterning method for TFT fabrication. The current AMLCD fabrication technique uses multi-step photolithographic masking, deposition and etching. This fabrication is expensive. Current commercial laser printers can print over an area of 11X17 sq. in. with a resolution of 1800 dpi, which is equivalent to a design rule of 10.6 μm. Given the rapid development of laser printing, we see the potential for TFT patterning with a 5 μm design rule.

In this project we explored several possible electrophotographic patterning methods for TFT fabrication. One possibility is to directly print a patterned layer. The second possibility is to print a pattern as a mask for etching or print a shadow mask for photolithography. Still another possibility is to print a buried pattern for lift-off. Combining these printing methods enable a procedure for fabricating TFTs *without* photolithographic equipment.

Program Major Tasks

- Print TFT layers: shadow mask, metal lines, etch mask, buried layers
- Study laser printer technology, develop computer-generated TFT pattern for printing, determine the limit of feature size
- Select proper toner materials for shadow mask, metal line, etch mask and lift-off
- Device and process design
- Etching
- Device fabrication and measurement

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II. Introduction

The photolithographic patterning techniques used in AMLCD manufacturing were developed for the manufacturing of integrated circuits on silicon wafers, and are correspondingly expensive. The exposure process requires stitching, is slow now, and may become even slower as the AMLCD size increases. We explored direct-printing techniques for semiconductor patterning and for metallization. Such techniques could revolutionize the large-area capability and the throughput of the manufacture of the backplane for AMLCDs and other large-area displays. In our project we used laser printing.

Commercial laser printers already can print over an area of 11 x 17 sq. in. with a resolution of 1800 dpi, which is equivalent to a design rule of ~ 14.5 μm. Toner particles currently available have ~ 3 μm diameter, with long-term prospects of reaching a minimum size of ~ 1 nm by using fullerene (C_{60}) as the toner. The lateral resolution limit is set by the optical diffraction of a laser diode, which lies around 1 μm. The limit set by the photoconductor is comparable to its thickness, which is of the order of 10 to 20 μm at present. With smaller toner particles, the voltage across the photoconductor can be reduced, and so can be its thickness, promising an increase in resolution to allow design rules of 5 μm or less. This means that the laser-printing technique could be applied to the production of the backplane of large-area displays.

III. Major Research Achievements

1. Patterned a-Si:H, SiN and metal with toner masks, and used toner as etching masks and lift-off masks

We researched two approaches for pattern transfer. One was to print on the transfer papers or films commercially available for the patterning of printed-circuit boards. The pattern is then transferred again, from the paper to the a-Si:H covered glass substrate, by applying heat and pressure.

Our second approach was direct laser printing on the desired surface. In contrast to the preceding case, this procedure does not require additional transfer steps. Therefore, higher resolution is possible. Because in AMLCD technology glass is the substrate, glass must be fed through the laser printer. This means that a laser printer with a straight paper (i.e., substrate) path must be used, and that the glass must be flexible. Commercially, large area glass foils as thin as 30 μm are available. We used 30-50 μm thick, 8.5 in. x 11 in., glass foils. We printed thin-film transistor type patterns on glass foil or on the foil covered with thin films.

We demonstrated the selective etching of a-Si:H, SiN and metal with toner masks, and used toner lift-off masks. More experimental details were reported in our publications (ref. 5, 10, 11, 12)

2. Fabrication of TFTs using printing for all patterning steps, completely replacing photolithography

Both top gate and bottom gate TFTs were fabricated using *all toner patterning processing*.

A typical top-gate TFT fabrication process is as follows:

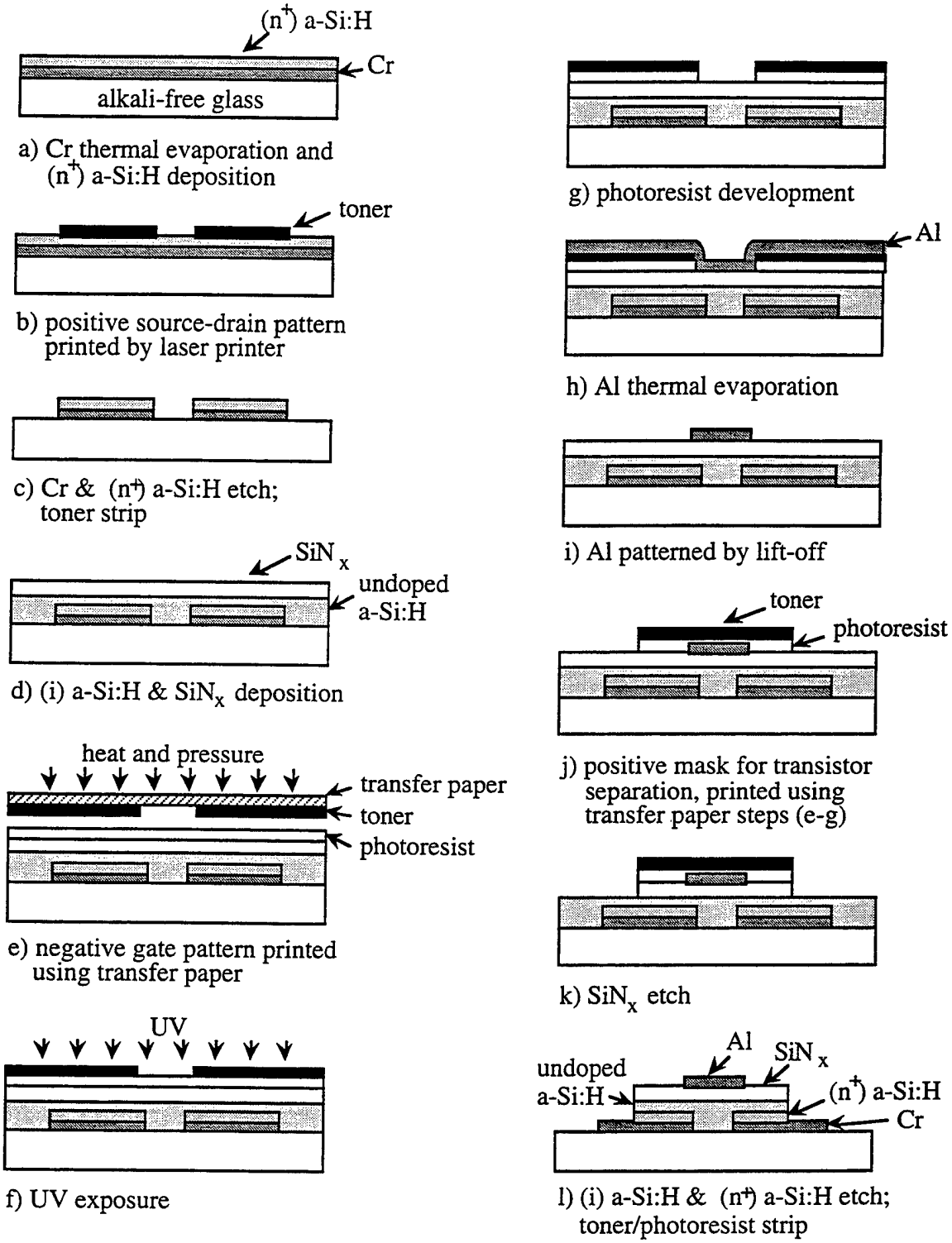

Fig. 1 Process of top-gate TFT using electrophotographic printing

The top-gate thin-film transistors (TFTs) were fabricated on 50-μm thick alkali-free glass foil (Schott # AF45). They have a simple staggered structure that requires only three patterning steps. These steps include direct printing for the first mask level, and transfer of toner masks for the higher levels. The entire process sequence is shown in Fig. 1. A 100-nm-thick layer of chromium (Cr) for the source-drain contacts is thermally evaporated onto the substrate. The Cr is patterned, and then the surface is cleaned. The 250-nm-thick channel layer of undoped a-Si:H and the 300-nm-thick gate insulator layer of silicon nitride (SiN_X) are deposited in a three-chamber plasma enhanced chemical vapor deposition system using dc and rf excitation, respectively. An identical layer of SiN_X (not shown) is deposited on the back side of the glass foil substrate to prevent etching of the glass by HF during further processing. We used the transfer paper technique for the second and higher mask levels. The printed side of the transfer paper and the glass substrate are brought in contact and are aligned under an optical microscope. Applying the proper amount of heat and pressure causes the toner to stick to the substrate. Following a water soak the transfer paper is peeled off the toner. When the toner is transferred in this way, it sticks well to semiconductor and insulator layers only if they are coated with photoresist. Using the toner as a mask the photoresist is exposed to UV-light and is developed. A layer of Cr is thermally evaporated and the gate electrode is patterned by lift-off. In the final step, which includes source/drain contact hole opening and transistor separation, we again use the transfer paper technique. We etched the SiN_X in 10% HF, and the a-Si:H in KOH solution. The photoresist and toner are stripped off with acetone and stripper.

Our bottom-gate, back-channel-etch TFTs need four patterning steps ("mask levels"). These steps include direct laser printing for the first mask level, and toner transfer for the higher levels. Recently, we are able to register two successive levels and use direct printing on more mask levels.

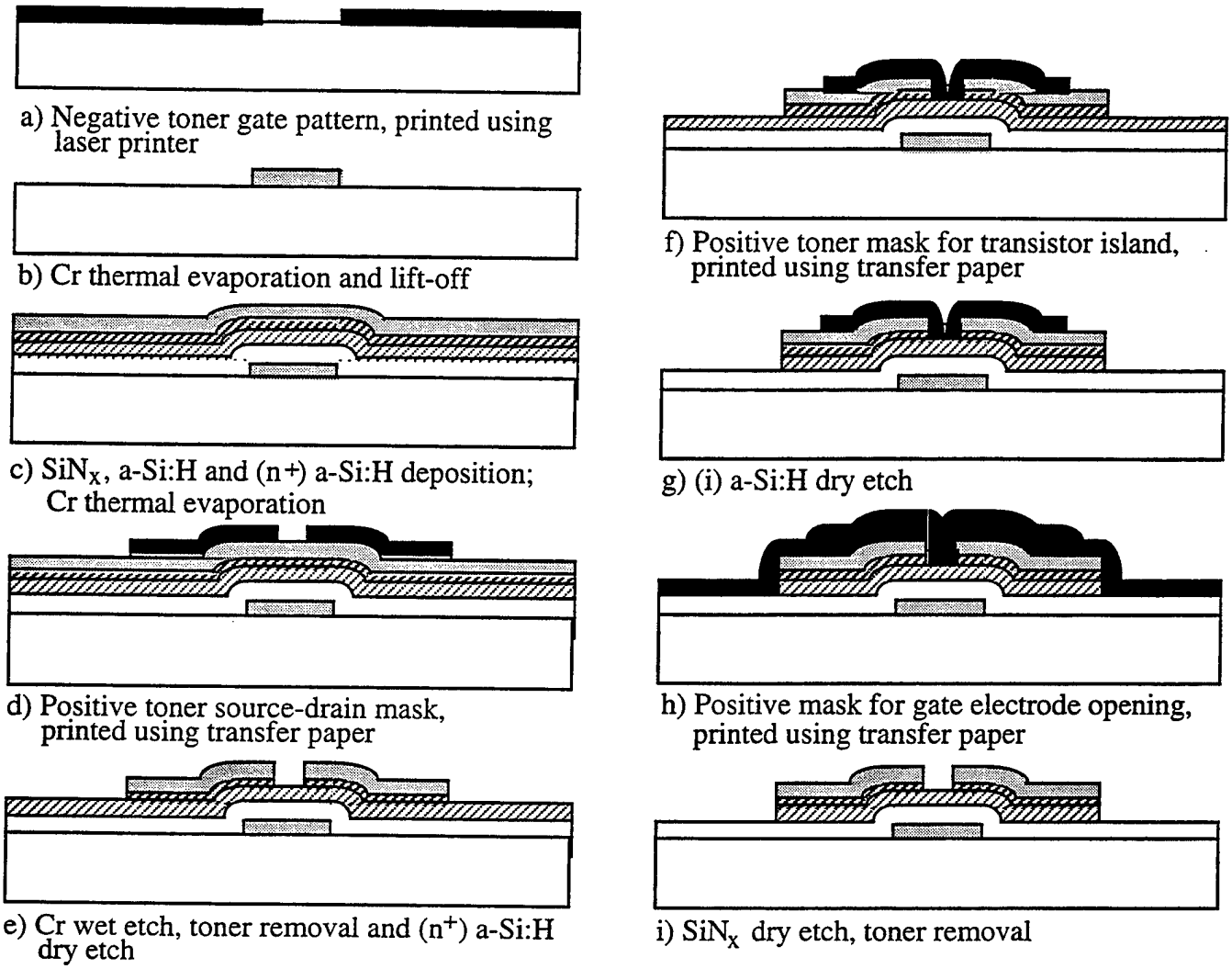

Fig. 2 Process of bottom-gate TFT using electrophotographic printing

The entire process sequence is shown in Fig. 2. First, we print a negative toner gate mask by running the glass foil through the laser printer. Then an ~ 100 nm thick Cr layer is thermally evaporated and the Cr/toner is lifted-off in toluene. We deposit a sequence of the following layers in a three-chamber plasma enhanced chemical vapor deposition system: ~ 410 nm of SiN_X, ~ 160 nm of undoped a-Si:H, and ~ 50 nm of (n^+) a-Si:H. An ~ 100 nm thick Cr layer is thermally evaporated. We print a positive source-drain toner pattern using transfer paper. Then the Cr layer is wet etched, the toner removed, and the (n^+) a-Si:H layer dry etched in

CF_4. Next, we print a positive toner mask for the TFT island formation, again using transfer paper. The undoped a-Si:H layer is dry etched in CF_4. Without stripping the mask, we print the final toner mask for the gate electrode opening, again using transfer paper. The SiN_x is dry etched in CF_4 and the toner removed. Because the nitride is etched only in the areas of the gate electrode pad it is not visible in Fig. 2(i). Finally, the TFTs are annealed for 30 min. in forming gas at 200°C to anneal out the radiation damage caused by the plasma during dry etching.

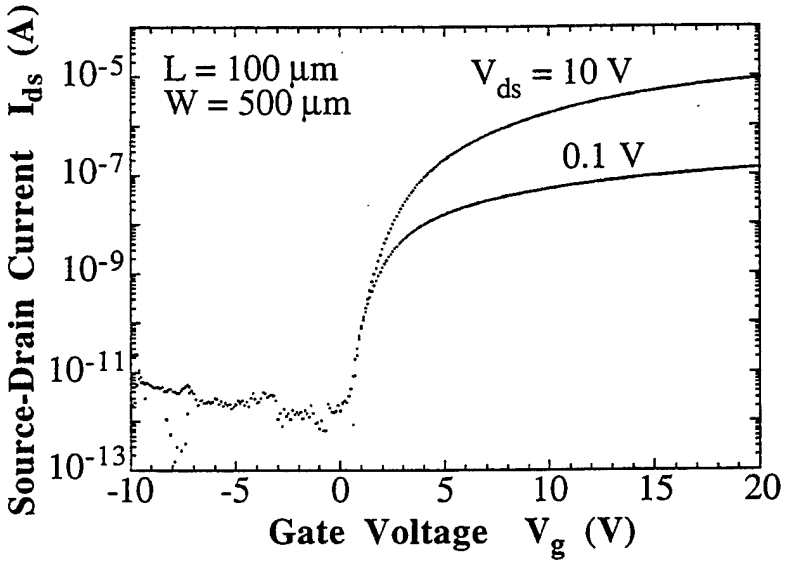

Fig. 3. TFT characteristic with all-printing processing

The characteristics of a transistor fabricated as described above are shown in Fig. 3. This figure shows the dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for V_{ds} = 0.1 V or 10 V. The off-current is < 10^{-14} A/µm and the on/off current ratio is ~ 10^7. We calculate an electron mobility of ~ 1 $cm^2 V^{-1} s^{-1}$. By making a-Si:H TFTs with electrical performance comparable to that of a-Si:H TFTs fabricated using conventional photolithography, we proved that electrophotographic printing can replace all conventional photolithographic steps in TFT fabrication. More experimental details are reported in our publications (see ref. 2, 4, 8, 9)

3. Research on very large AMLCD

Printing is particularly useful for very large displays. However, the size of the TFT backplane for active matrix liquid crystal displays (AMLCDs) is restricted by the RC delay of the bottom conductor, which in the standard inverted-staggered amorphous silicon TFT structure is the gate metal. To ensure good step coverage by the overlying insulator and semiconductor layers, the thickness of this gate conductor is limited to ~ 300 nm, and it must be kept narrow to provide a large pixel aperture. The maximum diagonal using low-conductivity metals is projected at ~ 40 inches.

In this project we have shown that the gate RC delay can be reduced considerably, and the AMLCDs be made correspondingly larger, by connecting the gate line through a few via holes to a bus run on the back side of the substrate. This bus can be much thicker than the gate line on the front side, because it is not part of the semiconductor structure.

We started with modeling and simulation. The new gate line powered through via holes is modeled as a modified RC delay line consisting of a cascade of two-port networks of finite pixels. Each two-port network represents one section of the line, which has via holes at both ends. The gate line pulse suffers distortion as it moves through the line. The distortion increases the rise time and delays the arrival of the gate pulse. The delay can cause the gate and data pulses to arrive at a pixel out of synchronization.

We used SPICE to simulate relationship between the maximum delay time and the physical parameters of the new structure. We found that the RC constant of pixel, the number of via holes L, the front-to-back resistance ratio K, and total number of pixels N are important factors for the determination of the delay time. A front-to-back resistance ratio K of 10 and 2 via holes in each line reduce the delay time to one seventh to one eighth.

Then we move on to device fabrication. We used 3 x 1.5 sq. in. 50 μm thick glass foil (Schott # AF 45) as the substrate for a-Si:H TFT fabrication. An 8x4 matrix of via holes was drilled from either one or from both sides using an ArF excimer laser. To demonstrate the feasibility

of laser drilling for third-generation AMLCD glass substrates, we also drilled holes into 0.5 mm thick Corning 7059 glass, again from either one or from both sides. Drilling from one side made funnel-shaped holes with entrance and exit diameters of ~ 40 μm and ~ 10 μm, respectively.

The bottom gate, back channel etched TFTs were fabricated using an all printed-toner patterning process. Each chromium gate pad on the front side of the substrate is collocated with a via hole for connection to a Cr bus run on the back side. The front-to-back connections through the via holes were made by two Cr evaporations, front and back, producing an ~ 1 kΩ through-resistance. In recent experiments we have reduced the through-hole resistance by 2 to 3 orders of magnitude with In filling or electroless-plated Cu. A top and two cross-sectional views of the TFT structure are shown in figure 4.

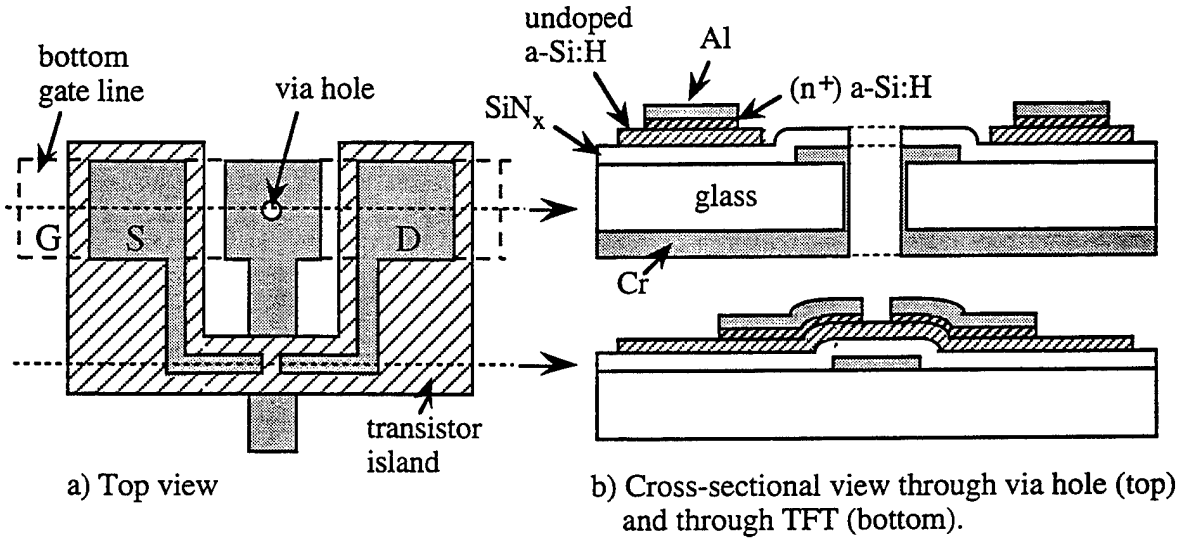

Fig. 4. Top view and cross-section view of TFT with via hole on substrate

The ON/OFF characteristics of a TFT addressed from the back side through a via connection are shown in figure 5. A photo of the TFT and via holes are also show in the figure. The off-current is ~ 1×10^{-14} A/μm, and the ON/OFF ratio is ~ 10^6. In the linear approximation at $V_{ds} = 1$ V we obtain $V_{Threshold} \sim 2.8$ V and an electron mobility of ~ 0.41 $cm^2 V^{-1} s^{-1}$. These

values are comparable to those of a-Si:H TFTs fabricated using conventional photolithography, and demonstrate the feasibility of the via hole concept (and of printed-toner masks).

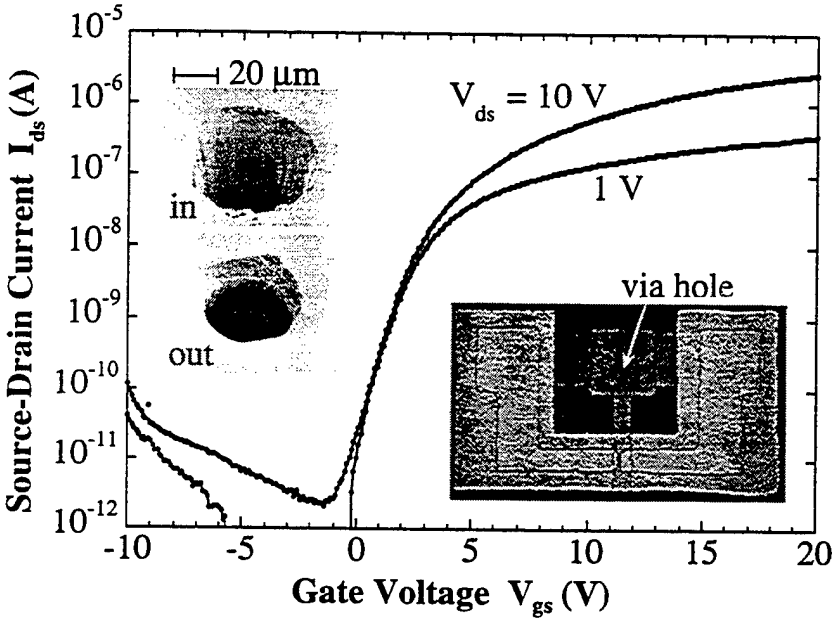

Fig. 5. Characteristics of TFT on via hole substrate. The transistor gates were addressed from the back side of the substrate through the via holes.

More details of modeling and experiments are reported in our publications (ref 1, 3, 6, 7)

IV. Review of Tasks and Results

In this section we review the tasks and results, emphasizing on the contents which are not covered in section III.

Task I . Printing TFT layers

Results:

We have successfully printed masks and patterned a-Si:H, SiN and metals. Cu lines were fabricated using printing-seeding-electroless plating procedure. In our original plan, metal powder was to be mixed with toner to print conducting patterns. However, the revised approach that we adopted has two advantages: one is that it avoids damaging the drum by metal particles. The other is that after plating the Cu film have a higher conductivity than copper powder mixed with toner. The detailed procedure is as follows:

A pattern is printed and transferred to glass as mentioned in the preceding section. Cu powder is spread as seeds. After heating, these seeds adhere to the pattern. Then electroless plating is carried out. The result shows that the Cu plates only on the pattern. Thus we proved that Cu conductor can grow selectively on a printed pattern. Figure 6 is a schematic of procedure.

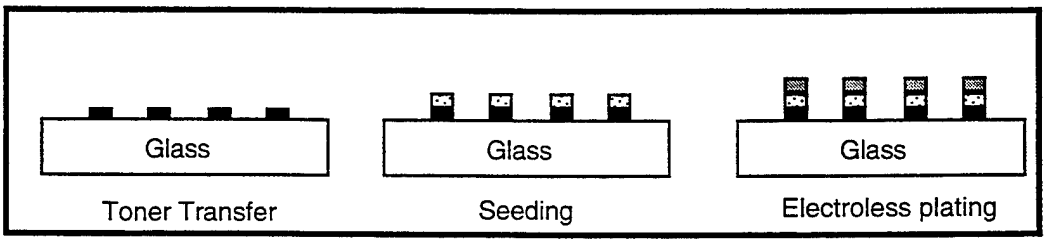

Fig. 6. Schematic of printing-seeding-electroless plating of Cu

Etching mask was printed, and thin films were etched by using a toner-photoresist double layer mask as well as a single toner layer. The toner must be post-baked to serve as a mask during the wet etching of a-Si:H in aqueous KOH solution. We experimented with a baking temperature of 160°C and baking times of 2 to 30 minutes in air; 30 min. gave the best result.

Buried layers were printed. These layers were used to pattern (by lift-off) the metal contact. We studied proper processing procedure for the lift-off of toners. We toner-patterned the glass foil. One sample of the toner was baked, while the other was not. Approximately 100 nm of chromium film was evaporated over these substrates. After lift-off, the toner was stripped with acetone. We found that the post-baking (at 120°C for one hour in air) gave better result.

We determined the toner topology with a surface profiler. The initial thickness and peak-to-valley roughness were ~ 12 μm and 3 μm, respectively. After post-baking the toner layer was ~ 9 μm thick, and was smooth. The post-baked toner is impermeable to the wet etchant. Fig. 7 shows a detail of the surface profile before and after the 30-minutes post-bake at 160°C in air. The small separate peak is from an isolated toner particle.

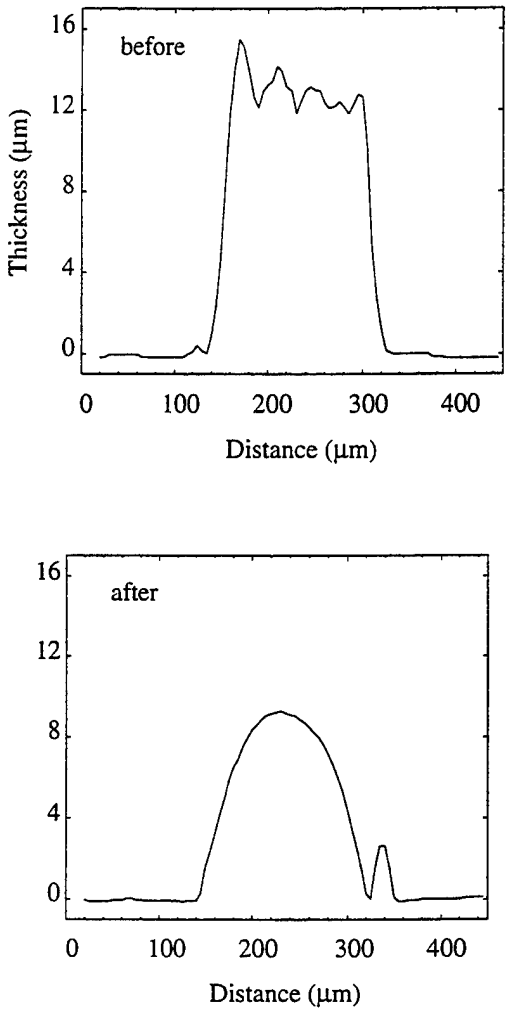

Fig. 7. Surface profile of the toner before and after post-baking at 160°C for 30 minutes. The post-bake trace shows an island made by a separate toner particle.

Task II. Laser printer technology

Results:

Computer generated mask patterns were printed. Software tools were evaluated. We looked into drawing programs, CAD tools, and PostScript programming. The capability of pattern generation, the convenience of usage and the cost of the software were evaluated.

We evaluated drawing programs which can manipulate bitmaps directly first. While such programs can generate desired pattern, it is quite slow for the computer and printer to process and print the pattern. We then looked into CAD tools. Although CAD tools with line width adjustment features exist, many can only adjust the line width to the screen pixel resolution (72 dpi), which is much wider than the resolution of laser printers (up to 1800 dpi today).

We found that the best way to generate pattern is to use PostScript programming. Most of the high resolution laser printers can print PostScript files. Since the pattern of the display panel is simple and repetitive, a short program can be used to generate the pattern. Furthermore, the line width can be adjusted easily. Using the PostScript program also can save the expense of the CAD tool. By adjusting the parameters in the program, one can easily generate a set of mask patterns for large area printing. Our pattern was printed by a 600 dpi laser printer. PostScript program for pattern generation has been developed.

The technology of high-resolution laser printers was assessed, and super-fine toner and potential novel toner materials were surveyed. Commercial laser printers already can print over an area of 11 x 17 sq. in. with a resolution of 1800 dpi, which is equivalent to a design rule of ~ 14.5 μm. The state of technology for high resolution laser printer has been studied and the commercial products have been surveyed. The resolution of a laser printer is basically determined by several factors. The dot size on the drum of laser printer is determined by the focusing of optical system and the number of the photons coming from the laser light. Thus the dot size can be manipulated by controlling the pulse width of the laser

diode. By shortening the pulse width, the amount of light hitting the drum can be reduced, thus a smaller toner-attracting area is resulted. The spin speed of the scan mirror and the speed at which the laser can turn on and off will determine how many dots can be drawn in a single line. Manipulate laser driving circuit to address more horizontal dot sizes could improve horizontal resolution. The degree of rotation of the drum determines the number of scan lines that can be drawn vertically. Thus slowing the drum's rotating speed could improve the vertical resolution. Current high-resolution commercial laser printers combine these approaches.

Toner particles currently available have ~ 3 μm diameter, with long-term prospects of reaching a minimum size of ~ 1 nm by using fullerene (C_{60}) as the toner. The lateral resolution limit is set by the optical diffraction of a laser diode, which lies around 1 μm. The limit set by the photoconductor is comparable to its thickness, which is of the order of 10 to 20 μm at present. With smaller toner particles, the voltage across the photoconductor can be reduced, and so can be its thickness, promising an increase in resolution to allow design rules of 5 μm or less. This means that the laser-printing technique could be applied to the production of the backplane of large-area displays.

We also studied the throughput of electrophotographic printing. In early stage of this program, an old Mac was used to generate the pattern, using drawing programs which manipulate bitmaps. We found that it takes very long (about one hour) to print the first copy of a computer designed mask pattern. The problem has been identified as the memory capacity of printer and computer, and the speed of the computer microprocessor. On a 8"X11" surface, a 600 dpi printer prints ~$32X10^6$ dots. Thus the demand on memory is high, if bitmap technology is used. Using a new computer and the PostScript program to generate patterns drastically reduced the first-copy printing time to less than one minute.

We also found that when multi-copy printing is used, the following copies (2nd copy, 3rd copy, etc.) come out in very short time (determined by the printer specifications, for the HP LaserJet 4M we used the speed is about 4 pages/min). This speed is not related to the programming technique, but rather is determined by the printer specifications. In fact,

commercial laser printer can easily reach a high printing speed (e.g., the printer for our computer network can print 20 page/min). Furthermore, because of the low cost of the printer, multiple printers can be used. Thus we conclude that throughput of laser printing is good.

Task III. Toner material

Results:

Proper toner (super-fine toner) was identified. Toner was used as etch mask, replacing the photoresist. Buried layer was printed with toner, and lift-off was used to pattern metal.

While the commercial toner works well in all these processing steps, a finer toner size is desired for high resolution printing. We think the long-term prospects is to use fullerene (C_{60}) as the toner, which can reach a minimum size of ~ 1 nm.

Task IV. Device and process design

Results:

We designed both top-gate and bottom gate TFT structures. postscript program was used to generate mask patterns for the TFTs. All processing steps (deposition, etching, mask printing) are tested, TFTs were fabricated. The details are reported in section III.

Task V. Etching

Results:

Two etchants (KOH, HF) for wet etching were tested. Dry etching (plasma etching) was also developed and used in TFT fabrication. More details are reported in section III.

Task VI. Doping and Crystallization

Our original plan was to use crystallized doping layers. However, after some experimentation, we decided to use amorphous doped layer instead. Mainly because that according to some literature, leakage current might increase in the TFT for crystallized materials.

Task VII. Device fabrication and measurement

Results:

Fabricated TFTs with all patterning done by printing instead of photolithography, with both top gate and bottom gate TFT structures. TFTs were evaluated. The results showed that the electrical performance of toner patterned TFTs is comparable with the TFTs fabricated using standard photolithography. More details are reported in section III.

V. Conclusions

We successfully accomplished all major tasks of this program, with following major achievements:

We demonstrated a novel patterning technique for thin-film electronics, which relies on electrophotography and flexible glass foil substrates. We described the direct printing of toner on glass foil and on a-Si:H coated foil, the use of this toner as an etch mask for a-Si:H, and in the patterning of Cr by lift-off.

We demonstrated the fabrication of amorphous silicon thin-film transistors in a process where all pattern definition steps use electrophotographic toner masks. While the process needs improvements, it already combines a drastic reduction of process steps with roll-to-roll type printing technique and electronic pattern generation. We view this combination as a powerful tool for developing large-area electronics.

We demonstrated a technique for increasing the size of AMLCD backplanes by reducing the gate RC delay. This technique consists of addressing the gates through via hole connections. Analysis shows that even a small number of via holes can have a large effect. An array of a-Si:H transistors was made on the 50 μm glass foils with via holes, using the new process where all pattern definition steps rely on electrophotographically printed toner masks. Thus we have demonstrated a new technology for RC gate delay reduction of particular benefit to large-area displays.

Two proposals on the further research have been submitted to DARPA.

VI. Appendix

Twelve papers reporting on the research results of this project were published. Re-prints are attached in this appendix. Support from DARPA/WPAFB is acknowledged.

Journal publications

1 "Modeling of Gate Line Delay in Very Large Active Matrix Liquid Crystal Displays", Q. Zhang, D.S. Shen, H. Gleskova and S. Wagner, *IEEE Tran. Electron Devices,*, Vol. 45, p. 343, 1998

2. "Photoresist-free Fbrication Process for a-Si:H TFTs", H. Gleskova, S. Wagner and D.S. Shen, *J. Non-Crystalline Solids*, to be published

3. "Via Hole Technology for Thin Film Transistor Circuits", H. Gleskova, S. Wagner, Q. Zhang and D.S. Shen, *IEEE Electron Device Lett.*, Vol. 18, p. 523, 1997

4. "Electrophotographically Patterned Thin Film Transistors", H. Gleskova, R. Konenkamp, S. Wagner and D.S. Shen, *IEEE Electron Device Lett.*, Vol. 17, p. 264, 1996

5. "Electrophotographic Patterning of Thin-Film Silicon on Glass Foil", H. Gleskova, S. Wagner and D.S. Shen, *IEEE Electron Device Lett.*, Vol. 16, p. 418, 1995

Conference publications

6. "Flexible Glass Substrates with Via Holes for TFT Backplane", H.Gleskova, E.Y. Ma, S.Wagner and D.S. Shen, 1997 Int. Workshop on AMLCD, Kobe, Nov. 1997, to be published.

7. "Via hole addressed TFT and process for large-area a-Si:H electronics", H. Gleskova, S. Wagner and D.S. Shen, *MRS Symp. Proc.*, April, 1997, to be published

8. "A-Si:H TFT Fabricated by Electrophotographic Printing", H. Gleskova, E.Y. Ma and S. Wagner and D.S. Shen, *Dig. Tech. Papers, 1996 Display Mfg. Technical Conf.*, SID, pp. 97, 1996

9. "a-Si:H TFTs Patterned Using Printed Toner", H. Gleskova, S. Wagner and D.S. Shen, *MRS Symp. Proc.*, Vol 426, 1996

10. "Patterning of a-Si:H by Laser Printing", D.S. Shen, H. Gleskova and S. Wagner, *Digest of Techn. Papers of SID Int. Symp.*, (Ed. Jay Morreale), SID, Santa Ana, CA, pp. 587, 1995

11. "Electrophotographic Patterning of a-Si:H", H. Gleskova, S. Wagner and D.S. Shen, *Proc. AMLCD's '95,* Lehigh University, pp. 16, 1995

12. "Electrophotographic Patterning of a-Si:H", H. Gleskova, S. Wagner, and D.S. Shen, *MRS Symp. Proc.*, Vol. 377, 1995

Other: In the following publications, partial support from DARPA/WPAFB are acknoledged.

13. "Transient Photocurrent in Hydrogenated Amorphous Silicon and Implications for Photodetector Devices", D.S. Shen and S. Wagner, *J. Appl. Phys.*, Vol. 79, p. 794, 1996

14. "Numerical Modeling of the Dependence of the Steady State Photoconductivity in Hydrogenated Amorphous Silicon on the Rate of Carrier Generation", D.S. Shen and S. Wagner, *J. Appl. Phys.*, Vol. 78, p. 278, 1995

Another paper, entitled ""Numerical Calculation of Gate Line Delay in Very Large Active Matrix Liquid Crystal Display with Via Holes", is submitted for publication in *IEEE Tran Circuits and Systems*. The paper is accepted, but not published yet.

Electrophotographic Patterning of Thin-Film Silicon on Glass Foil

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Abstract—**We report the patterning of thin films of amorphous silicon (a-Si:H) using electrophotographically applied toner as the etch mask. Using a conventional xerographic copier, a toner pattern was applied to 0.1 μm thick a-Si : H films deposited on $\sim$50 μm thick glass foil. The toner then served as the etch mask for a-Si : H, and as the lift-off material for the patterning of chromium. This technique opens the prospect of roll-to-roll, high-throughput patterning of large-area thin-film circuits on glass substrates.**

I. Introduction

LARGE-AREA electronics, based mostly on thin-film silicon, is under rapid development. 40 × 120-cm^2 solar panels [1] and 21-inch-diagonal active-matrix liquid-crystal displays [2] illustrate this new era of semiconductor technology. Much of the present-day manufacture of thin-film electronics is derived from integrated circuit fabrication. A principal factor in the wide use of integrated circuits has been their low cost, which is a consequence of their high functional density achieved by miniaturization. The path of miniaturization by definition cannot be taken to reduce the cost-per-function of large-area electronics [3], [4]. Instead, new materials and processing techniques are needed, such as metal foil [5] and plastic substrates [6], high deposition rates [7], and the low thermal budgets associated with hydrogenated amorphous silicon (a-Si : H). In this letter we describe a promising step toward the rapid and continuous processing of light-weight, large-area circuits, made by experimenting with the novel combination of a material, foil glass, with a processing technique, electrophotographic printing.

II. Experimental

Commercial laser printers can print over an area of 11 × 17 sq. in. (28 × 43 cm^2) with a resolution of 1800 dots per inch (dpi), which is equivalent to a design rule of $\sim$14.5 μm. Much higher resolution is possible, because the optical diffraction limit of laser diodes lies around 1 μm. The diameter of the toner particles, which is $\sim$3 μm at present, could be reduced to as little as 1 nm by using fullerene (C_{60}) [8]. The resolution set by the photoconductor thickness is comparable to its thickness, which currently is of the order of 10–20 μm. With smaller toner particles, the voltage across the photoconductor can be reduced, and so can be its thickness, thus promising an increase in resolution to allow design rules of 5 μm or less. This means that laser-printing could be applied to the production of thin-film electronics, i.e., the back plane of large-area displays.

Using laser-printed (or photocopied) toner as the etch mask requires the following steps: 1) pattern generation; 2) printing of the pattern on a film/substrate combination compatible with laser printing; and 3) selective etching. The toner also can substitute for photoresist in the lift-off technique. We describe both processes here. In a third process, the toner serves as a seed for the deposition of metal; this technique is reported elsewhere [9].

Drawing programs that manipulate bitmaps easily can generate patterns, but due to the large number of pixels, they demand very high memory capacity from the computer and the printer. Computer-aided design tools with linewidth adjustment features exist. However, many can adjust the line width only to the screen pixel resolution (72 dpi). We found that the best way to generate patterns is by PostScript programming. The line width can be adjusted easily, and the printing time is short. We generated patterns with a line width of $\sim$170 μm, corresponding to 150 dpi resolution.

Because the substrate must be fed through the laser printer, we introduced glass foil. Besides flexibility, glass foil offers the advantages of being lightweight and thin, and potentially, of roll-to-roll processing. Glass foils as thin as 30 μm are available commercially. We used 50 μm thick glass foil cut to 8.5 × 11 sq. in. [10]. A laser printer with a straight paper (i.e., substrate) path must be used. To lessen the replacement cost risked by the printing experiments reported here, we substituted a photocopier for the laser printer. We printed thin-film-transistor type patterns either directly on glass foil, or on foil on which we had deposited $\sim$100 nm thick layers of a-Si : H by plasma-enhanced chemical vapor deposition (PECVD) [11].

III. Results and Discussion

The quality of printing and pattern transfer can be evaluated from Fig. 1. In Fig. 1(a) a detail of the 150 dpi pattern is shown printed on paper with a 600 dpi laser printer; this print was used as the original in the subsequent photocopying on glass foil. Fig. 1(b) and (c) shows the same detail photocopied on paper, and on uncoated glass foil, respectively. Even though the original pattern was distorted by the photocopying, the quality of print on the glass is comparable to that on the paper.

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IEEE Log Number 9414365.

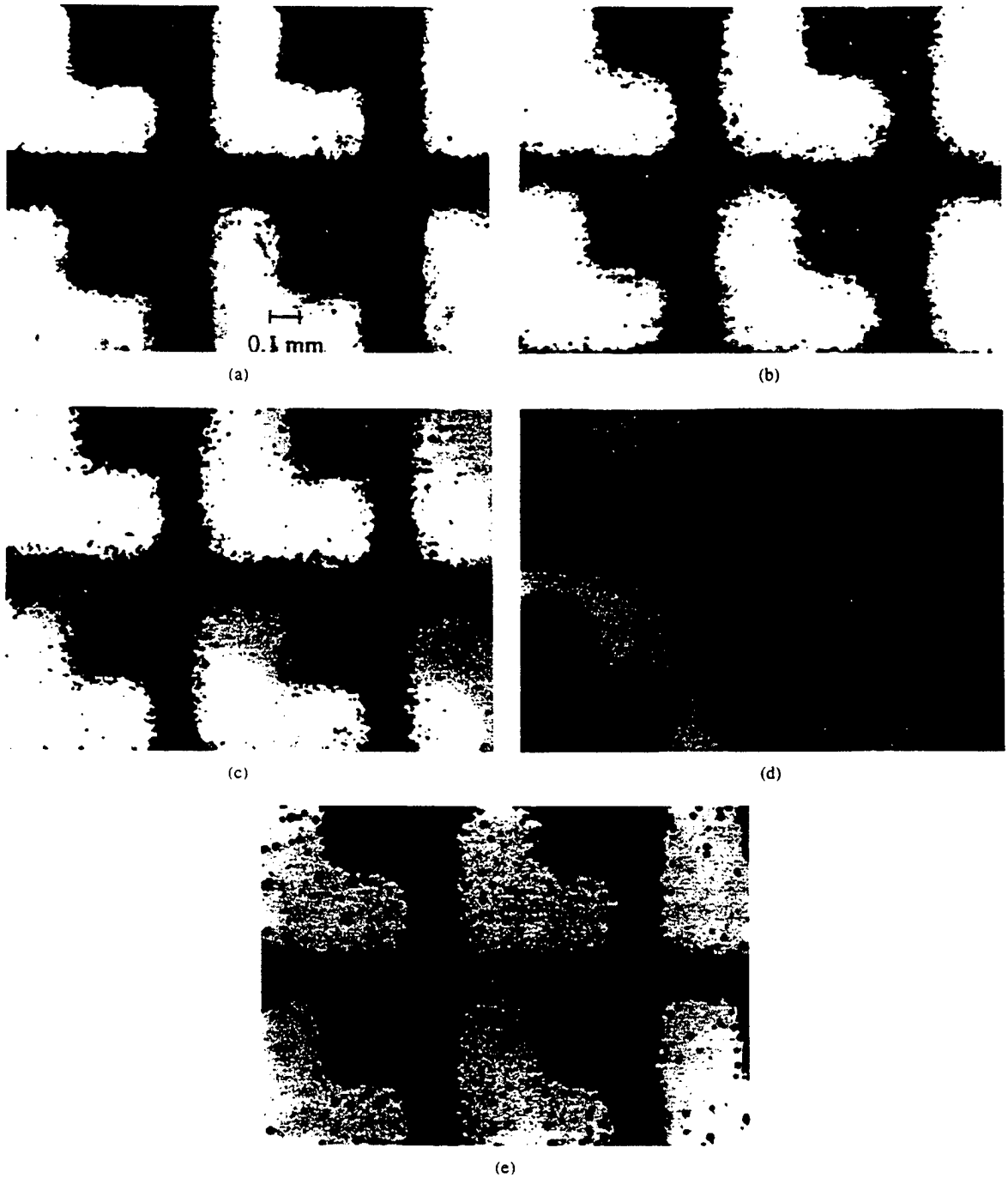

Fig. 1. Magnified detail of the 150 dpi pattern after (a) laser-printing at 600 dpi on paper to make the original for further photocopying; (b) photocopying on regular paper; (c) photocopying on glass foil; (d) patterning of a-Si : H (bright areas) by wet etch and strip; and (e) patterning of Cr (bright) by lift-off.

The glass had been cleaned with Micro laboratory cleaner before printing. The entire 8.5 × 11 sq. in. glass sheet can be seen in Fig. 2.

We used the same procedure for printing the pattern directly on a-Si : H deposited on the foil. The toner must be post-baked to serve as a mask during the wet etching of a-Si : H in aqueous KOH solution. We experimented with a baking temperature of 160°C and baking times of 2–30 min in air; 30 min gave the best result. We determined the toner topology with a surface profiler. The initial thickness and peak-to-valley roughness were ~11 μm and 3 μm, respectively. After post-baking the toner was 9 μm thick, and was smooth. The post-baked toner is impermeable to the wet etchant. A detail of the patterned a-Si : H is shown in Fig. 1(d). By future use of a high-resolution laser printer and of smaller toner particles, we expect to achieve better defined edges and cleaner patterns.

Fig. 1(e) demonstrates that the toner mask can also be used for lift-off patterning. We toner-patterned the glass foil as shown in Fig. 1(c). One sample of this toner was baked at 120°C for one hour in air, while the other was not. Approximately 100 nm of chromium film was evaporated over these substrates, and the toner was stripped with acetone. The post-baking gave the better result, which is the one shown in Fig. 1(e).

Fig. 2. Full view of the 8.5 × 11sq. in. glass sheet with a printed pattern.

The post-baked toner has the characteristics of a fused polymer, and thus, is not a source of particulate contamination. Therefore, we envisage application and post-baking of the toner in an enclosed processing tool to avoid clean room contamination with toner particles. We also foresee the use of conductive or photoconductive toners to prevent the buildup of electrochemical potentials during the wet etching of conductors, such as indium tin oxide. Furthermore, color pigment toners could be printed to form the front plane color filters.

IV. Conclusion

In summary, we demonstrated a novel patterning technique for thin-film electronics, which relies on electrophotography and flexible glass foil substrates. We described the direct printing of toner on glass foil and on a-Si : H coated foil, the use of this toner as an etch mask for a-Si : H, and in the patterning of Cr by lift-off.

Acknowledgment

The authors thank M. Nakata and Y. Chen for depositing a-Si : H on the glass foil.

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ELECTROPHOTOGRAPHIC PATTERNING OF a-Si:H

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ABSTRACT

A novel laser-printing method for the manufacturing of the backplane circuits of active-matrix liquid-crystal displays (AMLCD) is proposed and demonstrated. Xerographic toner is used as an etch mask for amorphous silicon (a-Si:H) and for the seeding of metal lines. We also demonstrate for the first time the direct-print patterning of silicon on ~ 50 μm thick glass foil.

INTRODUCTION

The photolithographic patterning techniques used in the AMLCD manufacturing were developed for the manufacturing of integrated circuits on silicon wafers, and are correspondingly expensive. Typically, six to nine thin film layers are used in the manufacturing of the backplane circuit, with photolithography required at each step [1]. The typical design rule for the channel of a thin-film transistor (TFT) is 3-5 μm [1]. Exposure by stepper requires stitching, which is accurate to ~ 1 μm [2], and is slow.

In order to decrease the price of AMLCDs, new alternative and cheaper methods for color filter manufacturing are being investigated. Among them are electrodeposition and printing, e.g. screen printing and offset printing [1]. We have been exploring direct-printing techniques for semiconductor patterning and for metallization. Such techniques could revolutionize the large-area capability and the manufacturing throughput of the backplane for AMLCDs and other large-area displays. In our current project we use laser printing.

Commercial laser printers already can print over an area of 11 x 17 sq. in. with a resolution of 1,800 dots per inch (dpi), which is equivalent to a design rule of ~ 14.5 μm. Toner particles currently available have ~ 3 μm diameter, with long-term prospects of reaching a minimum size of ~ 1 nm by using fullerene (C_{60}) as the toner [3]. The lateral resolution limit is set by optical diffraction of a laser diode, which lies around 1 μm. The limit set by the photoconductor is comparable to its thickness, which is of the order of 10 to 20 μm at present. With smaller toner particles, the voltage across the photoconductor can be reduced, and so can be its thickness, promising an increase in resolution to allow design rules of 5 μm or less. This means that the laser-printing technique could be applied to the production of the backplane of large-area displays.

In this paper we report our first experimental results on the patterning of a-Si:H by laser printing.

PATTERNING PROCEDURES AND RESULTS

To use a laser-printed toner as a photolithographic mask, the following steps are necessary: (1) pattern generation using computer software, (2) transfer of the pattern to the desired surface, and (3) selective etching.

Pattern generation

We evaluated computer software for pattern generation, considering the resolution of pattern generation, convenience of usage, and cost of software. We found that the best way for generating patterns is to use PostScript programming. Since the pattern of the display panel is simple and repetitive, a short program can be used. The line width can be adjusted easily, printing time is short, and the cost is low.

Pattern transfer, etching and additive growth

We have considered two approaches to pattern transfer. One is to print on the transfer papers commercially available for the patterning of printed-circuit boards [4]. This procedure is schematically shown in Fig. 1. Thin layers (100 - 400 nm) of a-Si:H or SiN_x are prepared by plasma-enhanced chemical vapor deposition (PECVD) on Corning 7059 glass substrates. The desired pattern, generated by computer, is printed on the transfer paper. The a-Si:H, deposited on glass, and the transfer paper are brought into contact, and heat and pressure are applied causing the toner to stick to the a-Si:H. The whole stack is then soaked in de-ionized (DI) water. During this soaking procedure the transfer paper peels from the toner. The result is that the printed toner covers the a-Si:H surface, while the rest of the a-Si:H surface is bare. This transfer also can be made onto a photoresist-covered a-Si:H film. If the pattern is transferred directly onto the semiconductor surface, it serves as a mask during etching. If the pattern is transferred onto the a-Si:H covered with photoresist, it serves as a mask during the UV-exposure of the photoresist. In such a case a standard procedure for the photoresist processing is used. The advantage over conventional photolithography is that this procedure does not require a mask aligner.

Because the surface of a-Si:H is very smooth, the pattern, when applied directly to a-Si:H surface, does not adhere well. However, the pattern transfers well to a-Si:H surfaces covered with photoresist.

Fig. 2(a) shows a detail of the TFT test pattern printed with a 600 dpi laser printer on the transfer paper. The thin line (gate) between source and drain is ~ 50 μm wide. Fig. 2(b) shows a similar TFT detail after the toner was transferred to the photoresist. Fig. 2(c) shows the same TFT detail after development of the photoresist. Fig. 2(d) shows the detail of Fig. 2(c) after a-Si:H was etched away in KOH solution at ~ 50°C and the photoresist was stripped off. We used a similar procedure for the patterning of SiN_x/glass and SiN_x/a-Si:H/glass structures. SiN_x was etched in 10% HF at room temperature.

As can be seen from Fig. 2, the contours of the pattern printed on the transfer paper lack smoothness and contrast. Toner particles can be found in places which should be free of them. The pattern becomes more distorted after pattern transfer to the photoresist. The final pattern etched into the a-Si:H (SiN_x) differs from the original one. In particular, the lines are thinner and the gaps wider than designed.

Our second approach is direct laser printing on the desired surface. In contrast to the preceding case, this procedure does not require additional transfer steps. Therefore, higher resolution should be possible. Because in AMLCD technology glass is the substrate, glass is fed through the laser printer. Large-area glass foils as thin as 30 μm are available commercially. We used 50 μm thick, 8.5 in. x 11 in., glass foils from Corning. The use of glass foils, in addition to their ability to run through the commercial photocopiers and laser printers, also offers the advantage of weight and thickness reduction. For our first demonstrations we substituted a photocopier for the laser printer. We printed patterns on the glass foil, or on ~ 100 nm thick a-Si:H deposited on the foil.

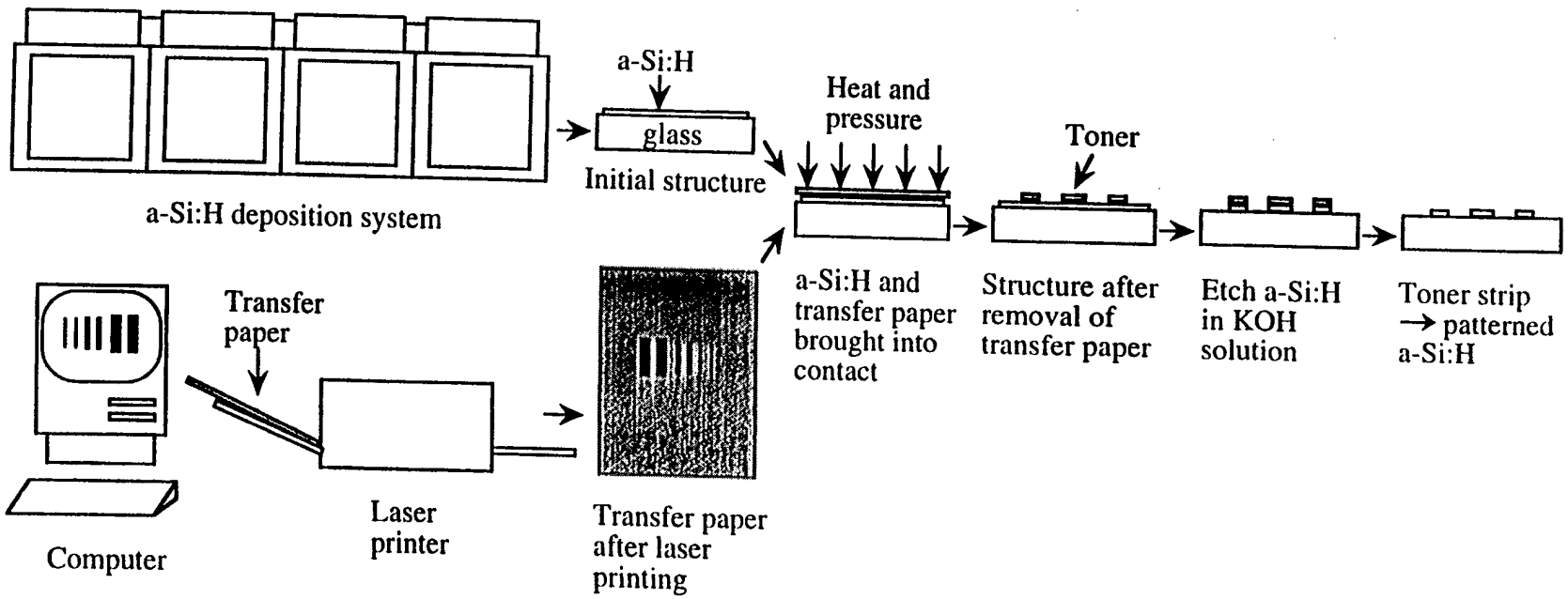

Fig. 1. Selective patterning of a-Si:H using transfer paper.

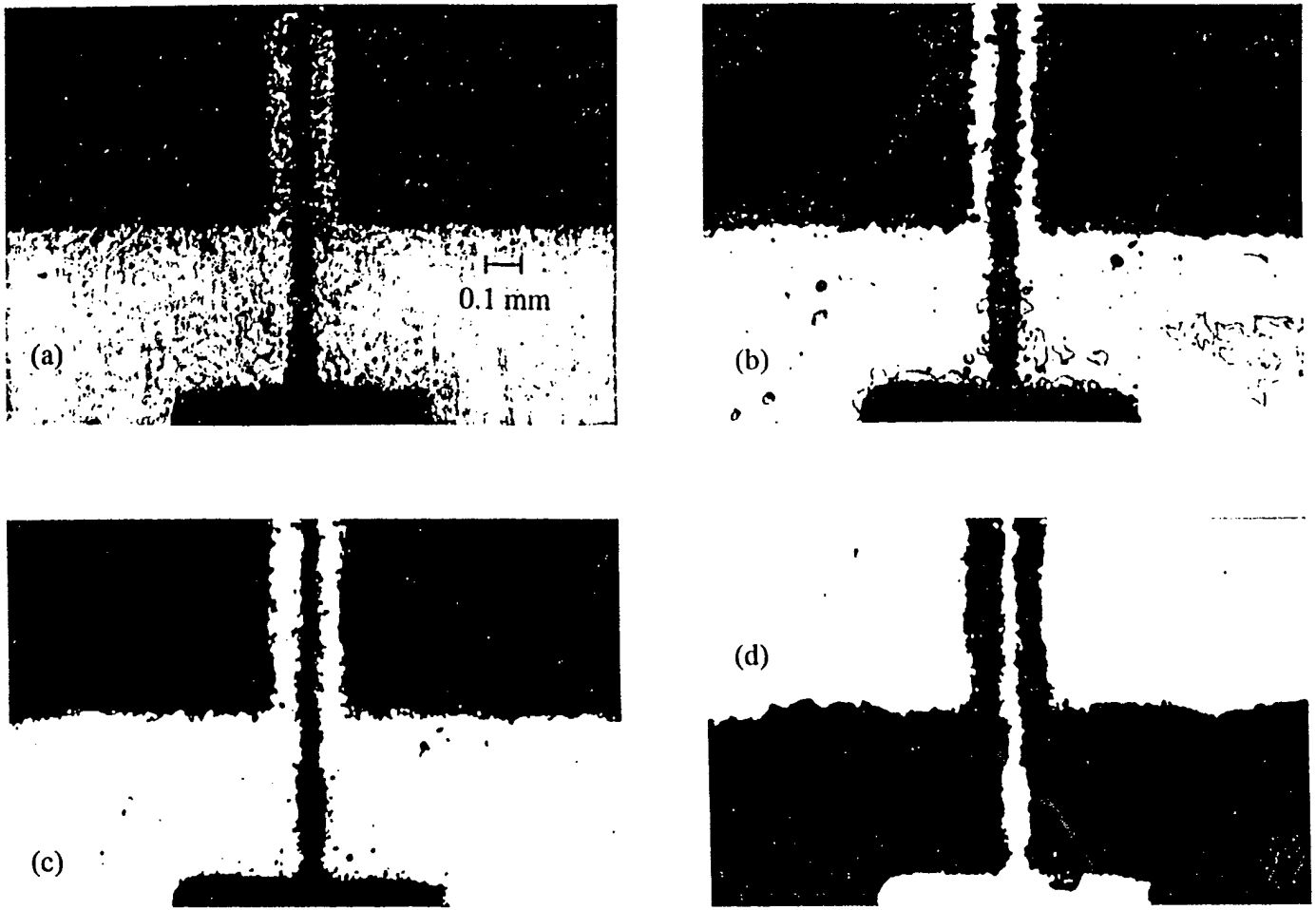

Fig. 2. Steps in the pattern transfer to a-Si:H deposited on a glass substrate. A magnified detail of a TFT test pattern is shown after:
(a) printing on the tranfer paper;
(b) transfer of the toner to the photoresist;
(c) development of the photoresist;
(d) a-Si:H etch and photoresist strip.

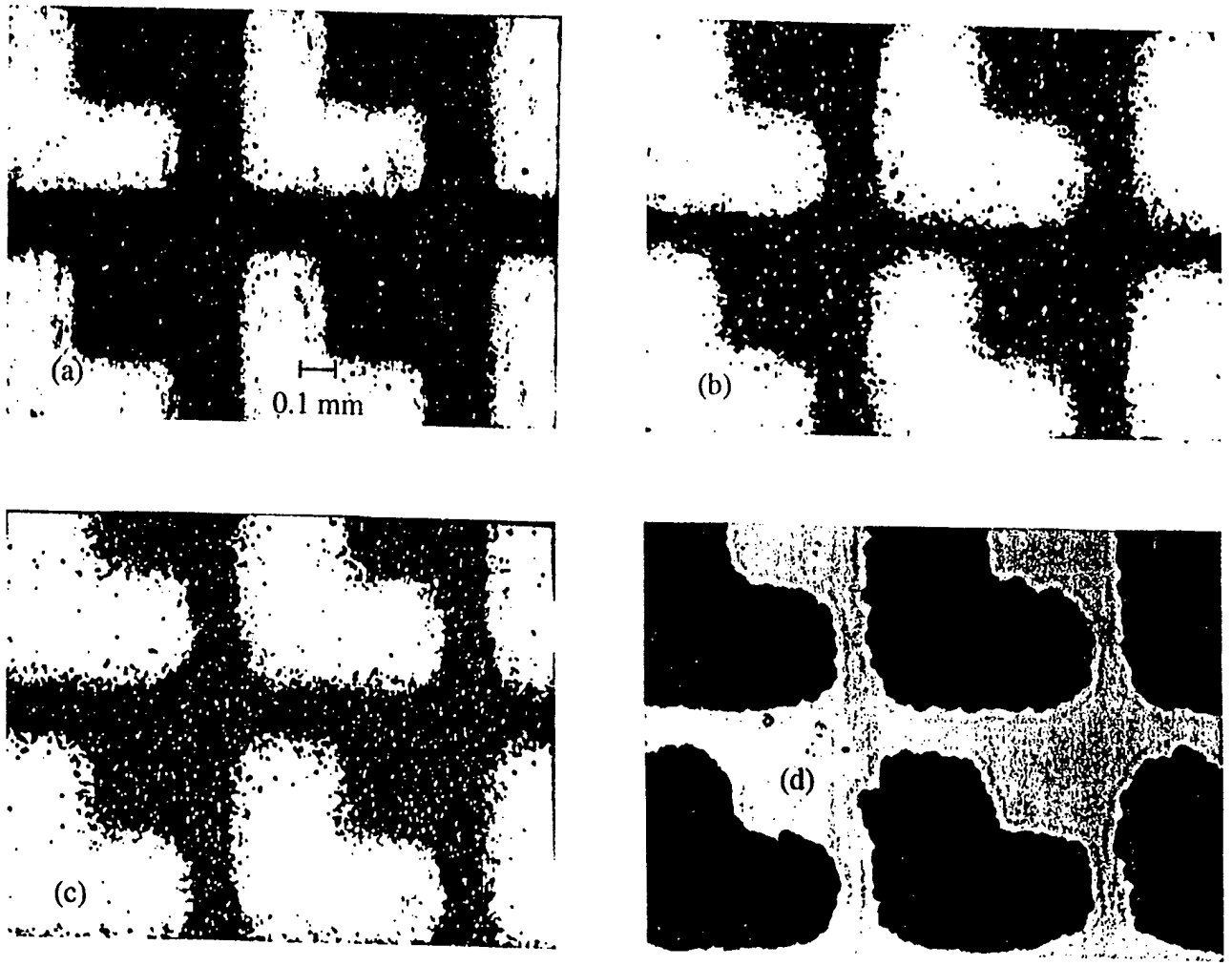

Fig. 3. Magnified detail of the 150 dpi pattern after:
(a) printing with a 600 dpi laser printer on regular paper, which then served as the original for photocopying;
(b) photocopying on regular paper;
(c) photocopying on glass foil;
(d) photocopying on the a-Si:H covered glas foil, followed by a-Si:H etch and toner strip.

Fig. 3(a) shows a detail of the 150 dpi pattern (line width ~ 170 μm) printed with a 600 dpi laser printer, which was used as the original for photocopying onto glass foil. Figs. 3(b) and 3(c) show the same detail photocopied on paper, and on glass foil, respectively. Note that even though the original pattern was distorted by the photocopying, the quality of the printout on the glass is comparable to that on the paper. The glass foil was cleaned with Micro laboratory cleaner, rinsed in de-ionized water, and nitrogen-dried before printing.

We used the same procedure for printing a pattern directly on a-Si:H deposited on glass foil. To serve as an mask during the wet KOH etching, the toner must be further baked outside the printer. We experimented with a baking temperature of 160°C, and found that of baking times from 2 to 30 minutes in air, 30 min. gave the best result. A detail of a-Si:H etched in KOH solution after this 30 min. bake is shown in Fig. 3(d).

For the additive growth of copper lines we employed a method of pattern transfer/seeding/ electroless plating as shown in Fig. 4. The printed pattern was transferred to glass by applying heat and pressure. The toner pattern on glass then was heated to a temperature such that copper powder adhered to the toner. The Cu-powder decorated toner pattern then was converted to continuous conductors by electroless plating.

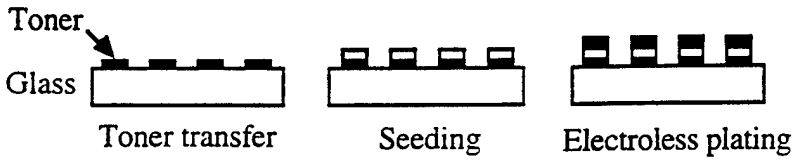

Fig. 4. Selective growth of metal lines.

SUMMARY

We demonstrated a novel laser-printing technique for the fabrication of the backplane of large-area displays. We evaluated and demonstrated (a) pattern generation using computer software, (b) pattern transfer using either direct laser printing on glass foil or on transfer paper, and (c) the ability of the toner to serve either as an etch mask for a-Si:H or for the seeding of metal lines. Thus we have demonstrated a new patterning technology for AMLCD manufacturing, which does not require photolithographic equipment.

ACKNOWLEDGMENT

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Patterning of a-Si:H by Laser Printing

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Abstract

A novel laser-printing method for the manufacturing of the backplane circuits of active-matrix liquid-crystal displays (AMLCD) is proposed and demonstrated. Xerographic toner is used as an etch mask for amorphous silicon (a-Si:H) and for the seeding of metal lines. We also demonstrate for the first time the direct-print patterning of silicon on flexible glass foil.

Introduction

The photolithographic patterning techniques used in the AMLCD manufacturing were developed for the manufacturing of integrated circuits on silicon wafers, and are correspondingly expensive. The exposure process requires stitching, is slow now, and may become even slower as the AMLCD size increases. We have been exploring direct-printing techniques for semiconductor patterning and for metallization. Such techniques could revolutionize the large-area capability and the throughput of the manufacture of the backplane for AMLCDs and other large-area displays. In our current project we use laser printing.

Commercial laser printers already can print over an area of 11 x 17 sq. in. with a resolution of 1,800 dpi, which is equivalent to a design rule of ~ 14.5 μm. Toner particles currently available have ~ 3 μm diameter, with long-term prospects of reaching a minimum size of ~ 1 nm by using fullerene (C_{60}) as the toner [1]. The lateral resolution limit is set by the optical diffraction of a laser diode, which lies around 1 μm. The limit set by the photoconductor is comparable to its thickness, which is of the order of 10 to 20 μm at present. With smaller toner particles, the voltage across the photoconductor can be reduced, and so can be its thickness, promising an increase in resolution to allow design rules of 5 μm or less. This means that the laser-printing technique could be applied to the production of the backplane of large-area displays.

In this paper we report our first experimental results on the patterning of a-Si:H by laser printing.

Experimental procedures

To use a laser-printed toner as a photolithographic mask the following steps are necessary: (1) pattern generation using computer software, (2) transfer of the pattern to the desired surface, and (3) selective etching.

Pattern generation

We evaluated computer software for pattern generation. We looked into drawing programs, which can manipulate bitmaps directly, CAD tools, and PostScript programming. The capability of pattern generation, the convenience of usage and the cost of the software were evaluated.

Pattern transfer

So far we have considered two approaches to pattern transfer. One is to print on the transfer papers or films commercially available for the patterning of printed-circuit boards [2]. The pattern is then transferred again, from the paper to the a-Si:H covered glass substrate, by applying heat and pressure. This procedure is schematically shown in Fig. 1. Thin layers (100 - 400 nm) of a-Si:H or SiN_x are prepared by PECVD on Corning 7059 glass substrates. The desired pattern is generated by computer and printed on the transfer paper. The a-Si:H, deposited on glass, and the transfer paper are brought into the contact, and heat and pressure are applied causing the toner to stick to the a-Si:H. The whole stack is then soaked in de-ionized (DI) water. During this soaking procedure the transfer paper peels from the toner, which adhered to the a-Si:H surface. The result is that the printed toner covers the a-Si:H surface, while the rest of the a-Si:H surface is bare. This transfer also can be made onto a photoresist-covered a-Si:H film. If the pattern is transferred directly on the semiconductor surface, it serves as a mask during etching. If the pattern is transferred on the a-Si:H covered with photoresist, it serves as a mask during the UV-exposure of the photoresist. In such a case a standard procedure for the photoresist processing is used. The advantage over conventional photolithography is that this procedure does not require a mask aligner and the photoresist can be flat exposed. For our experiments we selected AZ 5214E photoresist. In addition to a soft bake, prior to the wet etching, the photoresist was hard baked at 170°C for one hour.

Our second approach is direct laser printing on the desired surface. In contrast to the preceding case, this procedure does not require additional transfer steps. Therefore, higher resolution should be possible. Because in AMLCD technology glass is the substrate, glass must be fed through the laser printer. This means that a laser printer with a straight paper (i.e., substrate) path must be used, and that the glass must be flexible. Commercially, large area glass foils as thin as 30 μm are available. We used 50 μm thick, 8.5 in. x 11 in., glass foils from Corning. For our first demonstrations we substituted a photocopier for the laser printer. We printed

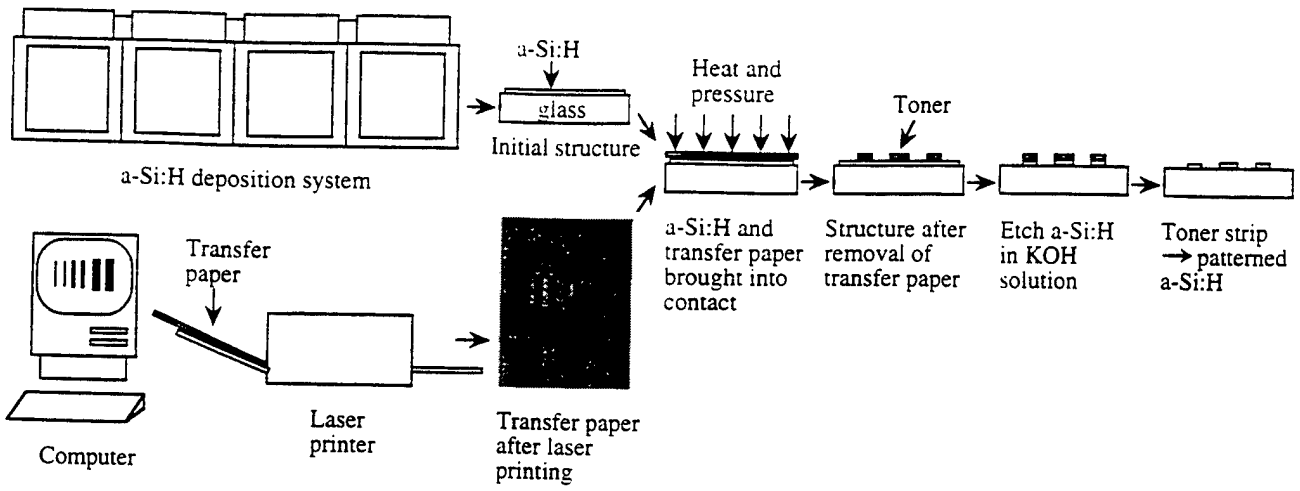

Figure 1. Selective patterning of a-Si:H using transfer paper.

thin-film transistor type patterns on glass foil or on the foil covered with ~ 100 nm thick layer of a-Si:H.

Selective etching and additive growth

We demonstrated the selective etching of a-Si:H semiconductor and the selective addition of metal on substrates patterned with toner as described above.

We toner-patterned and wet-etched the following layers: a-Si:H/glass, SiN_x/glass, and SiN_x/a-Si:H/glass. a-Si:H was etched in aqueous KOH solution at 40-50°C. SiN_x was etched in 10% HF at room temperature. The photoresist was stripped off in AZ 300T stripper heated to ~ 50°C.

For the additive growth of copper lines we employed a method of pattern transfer -- seeding -- electroless plating as shown in Fig. 2. The printed pattern was transferred to glass by applying heat and pressure. The toner pattern on glass then was heated to a temperature such that copper powder adhered to the toner. The Cu-powder decorated toner pattern then was converted to continuous conductors by electroless plating.

Experimental results and discussion

Pattern generation

Drawing programs which manipulate bitmaps can easily generate a test pattern. However, due to the large number of pixels, the memory capacity of the printer and computer has to be very high. CAD tools with line width adjustment features exist, however, many can only adjust the width to the screen pixel resolution (72 dpi), and some are expensive. We found that the best way for generating patterns is to use PostScript programming. All high resolution laser printers can print PostScript files. Since the pattern of the display panel is simple and repetitive, a short program can be used. The line width can be adjusted easily, printing time is short, and the cost is low.

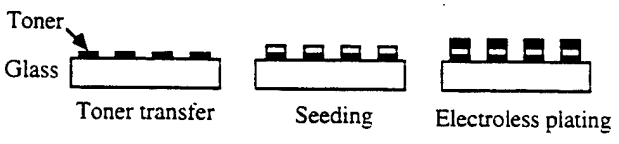

Figure 2. Selective growth of metal lines.

Pattern transfer using transfer paper

In this procedure the transfer paper was fed through a 600 dpi laser printer and a test pattern was printed on it. The test pattern contains a system of lines and rectangles which simulates the patterns needed for TFT production. Then the print side of the transfer paper was brought into the contact with a-Si:H deposited on glass substrate, or with a-Si:H covered with photoresist. Because the surface of a-Si:H is very smooth the pattern, when applied directly to a-Si:H surface, does not adhere. This inadequate adhesion produces pattern distortion which becomes a problem for small features. However, the pattern transfers well to a-Si:H surfaces covered with photoresist.

Fig. 3 shows a detail of the TFT test pattern printed with a 600 dpi laser printer on the transfer paper. The thin line (gate) between source and drain is ~ 50 μm wide. Fig. 4(a) shows a similar TFT detail after the toner was transferred to the photoresist. Fig. 4(b) shows the same TFT detail of the test pattern after development of the photoresist. Fig. 4(c) shows the TFT detail after a-Si:H was etched away in KOH solution and the photoresist was stripped off.

We used a similar procedure for the patterning of SiN_x deposited on glass. In this case, the KOH solution was replaced by 10% HF. Results similar to those shown in Fig. 4 were obtained.

Finally, we attempted to pattern SiN_x deposited on a-Si:H layer. In this case the AZ 300T stripper must be used with caution. If the temperature of the stripper is too low,

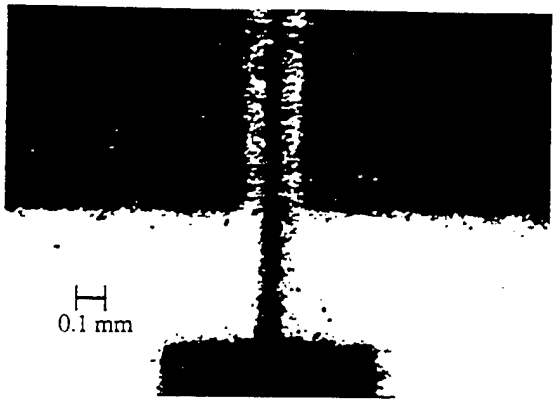

Figure 3. Magnified detail of a TFT test pattern after printing on the transfer paper.

the photoresist cannot be stripped. If the temperature is too high, the stripper etches the underlying layer of a-Si:H. We need to do further experiments to define the intermediate range of temperature in which the photoresist can be stripped while the underlying a-Si:H remains intact.

As can be seen from Fig. 3 and Fig. 4, the contours of the pattern printed on the transfer paper lack smoothness and contrast. Toner particles can be found in places which should be free of them. The pattern becomes more distorted after pattern transfer to the photoresist. The final pattern etched into the a-Si:H (SiN_x) differs from the original one. Especially, the lines are thinner and the gaps wider than designed.

Direct laser printing

The difficulties with pattern transfer can be avoided by printing directly on glass. Glass foils can run through a laser printer or photocopier without breaking. To test this technique we generated two sets of patterns, the first with a line width of ~ 170 μm, corresponding to 150 dpi resolution, and the second, with a line width of ~ 42 μm, corresponding to 600 dpi resolution. Fig. 5(a) shows a detail of the 150 dpi pattern printed with a 600 dpi laser printer which was used as the original for photocopying onto glass foil. Figs. 5(b) and 5(c) show the same detail photocopied on paper, and on glass foil, respectively. Note that even though the original pattern was distorted by the photocopying, the quality of the printout on the glass is comparable to that on the paper. Except for the regular cleaning procedure for the glass substrates, no surface preparation was used before printing on the glass.

We used the same procedure for printing a pattern directly on a-Si:H deposited on thin glass. To serve as an mask during the wet KOH etching, the toner must be further baked. We experimented with a baking temperature of 160°C, and the baking times from 2 to 30 minutes in air. 30 min. gave the best result. A detail of a-Si:H etched in KOH solution after the 30 min. bake is shown in Fig. 6.

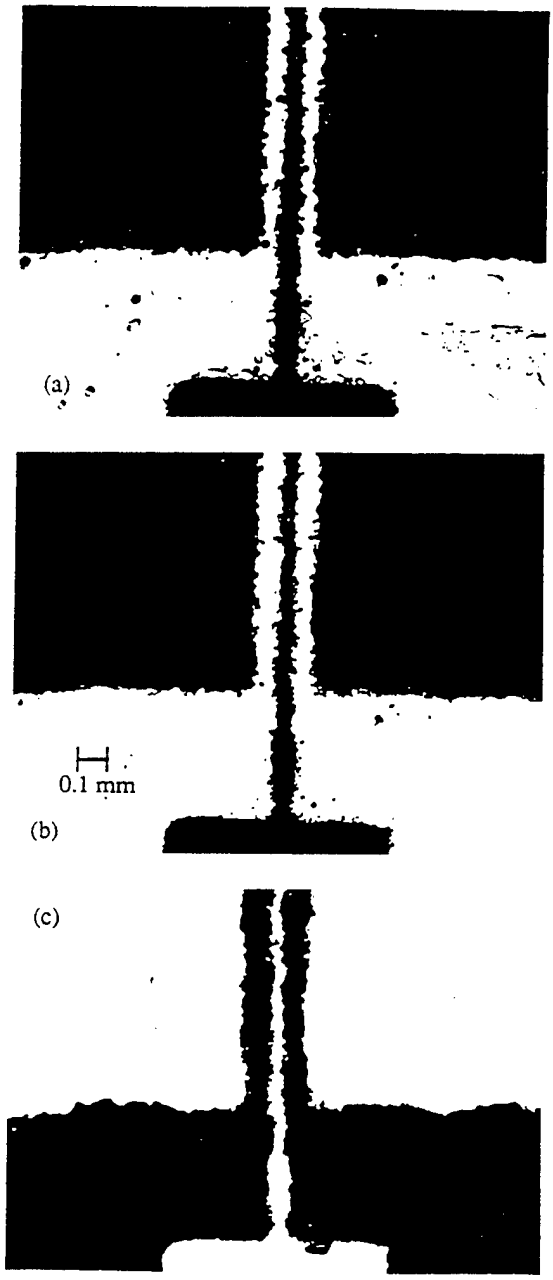

Figure 4. Steps in the pattern transfer to a-Si:H deposited on a glass substrate. A magnified detail of a TFT test pattern is shown after:
(a) transfer of the toner to the photoresist
(b) development of the photoresist
(c) a-Si:H etch and photoresist strip.

The patterns with 600 dpi lines could not be photocopied well either onto paper or onto glass due to the low resolution of the optics in the photocopier we used. Further experiments are necessary.

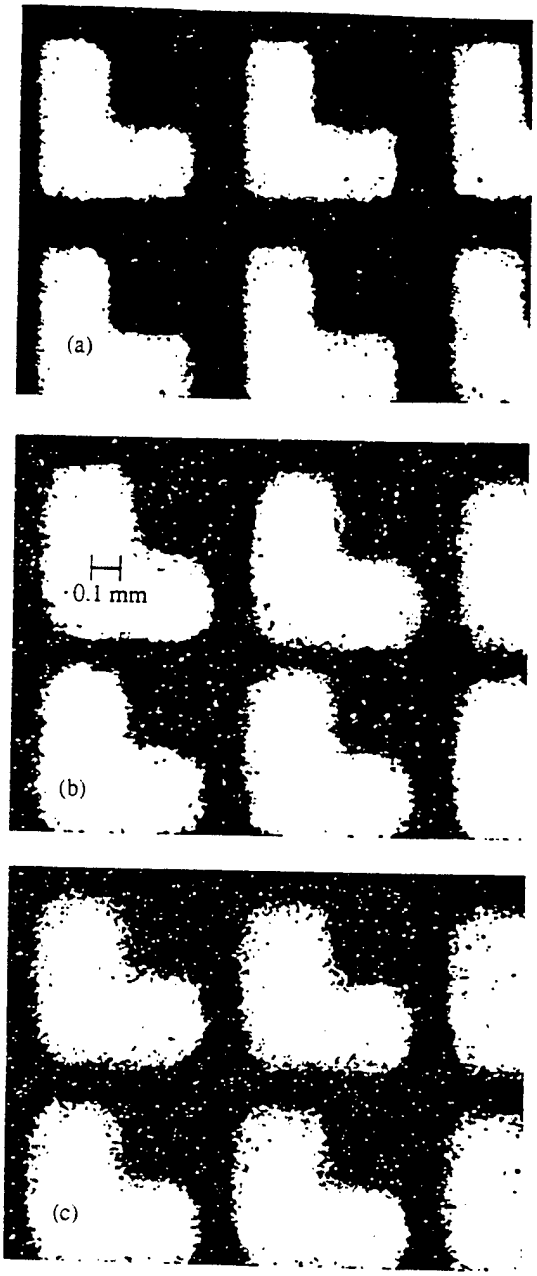

Figure 5. Magnified detail of the 150 dpi pattern after
(a) printing with a 600 dpi laser printer on regular paper, which then served as the original for photocopying.
(b) photocopying on regular paper
(c) photocopying on glass foil.

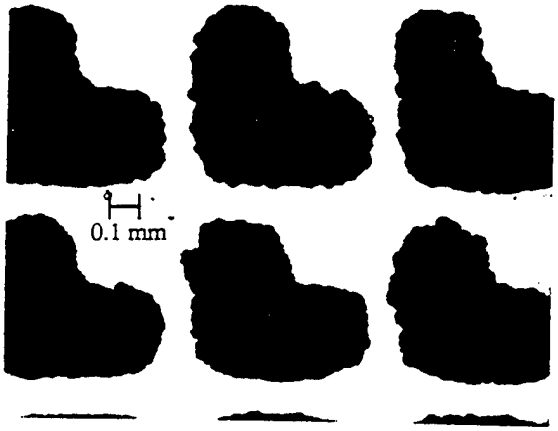

Figure 6. Magnified detail of Fig. 5 printed on a-Si:H/glass foil, after a-Si:H etch and toner strip.

Summary

We demonstrated a novel laser-printing technique for the fabrication of the backplane of large-area displays. We evaluated and demonstrated (a) pattern generation using computer software, (b) pattern transfer using either direct laser printing on glass foil or on transfer paper, and (c) the ability of the toner to serve either as an etch mask for a-Si:H or for the seeding of metal lines. Thus we have demonstrated a new patterning technology for AMLCD manufacturing, which does not require photolithographic equipment.

Acknowledgement

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* On leave from the Department of Solid State Physics, Comenius University, Bratislava, Slovakia.

1. US patent # 5,188,918 and US patent # 5,232,810.
2. Available from DynaArt Design, Lancaster, CA 93536 or from Techniks, Ringoes, NJ 08551.

Lehigh '95

ELECTROPHOTOGRAPHIC PATTERNING OF a-Si:H

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ABSTRACT

We report the patterning of thin films of amorphous silicon (a-Si:H) using electrophotographically applied toner as the etch mask. Using a conventional xerographic copier, a toner pattern was applied to 0.1 μm thick a-Si:H films deposited on ~ 50 μm thick glass foil. The toner then served as the etch mask for a-Si:H, and as the lift-off material for the patterning of chromium. This technique opens the prospect of roll-to-roll, high-throughput patterning of large-area thin-film circuits on glass substrates.

INTRODUCTION

Large-area electronics, based mostly on thin-film silicon, is under rapid development. 40x120-cm^2 solar panels [1] and 21-inch-diagonal active-matrix liquid-crystal displays [2] illustrate this new era of semiconductor technology. Much of the present-day manufacture of thin-film electronics is derived from integrated circuit fabrication. A principal factor in the widespread use of integrated circuits has been their low cost, which is a consequence of their high functional density achieved by miniaturization. The path of miniaturization by definition cannot be taken to reduce the cost-per-function of large-area electronics [3,4]. Instead, new materials and processing techniques are needed, such as metal foil [5] and plastic substrates [6], high deposition rates [7], and the low thermal budgets associated with hydrogenated amorphous silicon (a-Si:H). In this paper we describe a promising step toward the rapid and continuous processing of light-weight, large-area circuits, made by experimenting with the novel combination of a material, foil glass, with a processing technique, electrophotographic printing.

EXPERIMENTAL PROCEDURES AND RESULTS

Commercial laser printers can print over an area of 11x17 sq.in. (28x43 cm^2) with a resolution of 1,800 dots per inch (dpi), which is equivalent to a design rule of ~ 14.5 μm. Much higher resolution is possible, because the optical diffraction limit of laser diodes lies around 1 μm. The diameter of the toner particles, which is ~ 3 μm at present for common toners, and ~ 1 μm for specialized toners, could be reduced to as little as 1 nm by using fullerene (C_{60}) [8]. The resolution set by the photoconductor thickness is comparable to its thickness, which currently is of the order of 10 to 20 μm. With smaller toner particles, the voltage across the photoconductor can be reduced, and so can be its thickness, thus promising an increase in resolution to allow design rules of 5 μm or less. This means that laser-printing could be applied to the production of thin-film electronics, for example, the back plane of large-area displays.

Using laser-printed (or photocopied) toner as the etch mask requires the following steps: (1) pattern generation; (2) printing of the pattern on a film/substrate combination compatible with laser printing; and (3) selective etching. The toner also can substitute for photoresist in the lift-off technique. We describe both processes here. In a third process the toner serves as the seed for the deposition of metal; this technique is reported elsewhere [9].

Drawing programs that manipulate bitmaps easily can generate patterns, but due to the large number of pixels they demand very high memory capacity from the computer and the printer. Computer-aided design tools with linewidth adjustment features exist. However, many can adjust the line width only to the screen pixel resolution (72 dpi). We found that the best way for generating patterns is by PostScript programming. The line width can be adjusted easily, and the printing time is short. We generated patterns with a line width of ~ 170 μm, corresponding to 150 dpi resolution.

Because the substrate must be fed through the laser printer, we introduced glass foil. Besides flexibility, glass foil offers the advantages of light weight, of being thin and, potentially, of roll-to-roll processing. Glass foils as thin as 30 μm are available commercially. We used 50 μm thick glass foil cut to 8.5 in. x 11 in. [10]. A laser printer with a straight paper (i.e., substrate) path must be used. To lessen the replacement cost risked by the printing experiments reported here, we substituted a photocopier for the laser printer. We printed thin-film-transistor type patterns either directly on glass foil, or on foil on which we had deposited ~ 100 nm thick layers of a-Si:H by plasma-enhanced chemical vapor deposition (PECVD) [11].

The quality of printing and pattern transfer can be evaluated from Fig.1. In Fig. 1(a) a detail of the 150 dpi pattern is shown printed on paper with a 600 dpi laser printer; this print was used as the original in the subsequent photocopying on glass foil. Figs. 1(b) and 1(c) show the same detail photocopied on paper, and on uncoated glass foil, respectively. Even though the original pattern was distorted by the photocopying, the quality of print on the glass is comparable to that on the paper. The glass had been cleaned with Micro laboratory cleaner before printing. The entire 8.5 in. x 11 in. glass sheet can be seen in Fig. 2.

We used the same procedure for printing the pattern directly on a-Si:H deposited on the foil. The toner must be post-baked to serve as a mask during the wet etching of a-Si:H in aqueous KOH solution. We experimented with a baking temperature of 160°C and baking times of 2 to 30 minutes in air; 30 min. gave the best result. A detail of the patterned a-Si:H is shown in Fig. 1(d). Through future use of a high-resolution laser printer and of smaller toner particles we expect to achieve better defined edges and cleaner patterns.

Fig. 1(e) demonstrates that the toner mask can also be used for lift-off patterning. We toner-patterned the glass foil as shown in Fig. 1(c). One sample of this toner was baked at 120°C for one hour in air, while the other was not. Approximately 100 nm of chromium film was evaporated over these substrates, and the toner was stripped with acetone. The post-baking gave the better result, which is the one shown in Fig.1 (e).

We determined the toner topology with a surface profiler. The initial thickness and peak-to-valley roughness were ~ 12 μm and 3 μm, respectively. The roughness is consistent with a toner particle size of 3 μm. After post-baking the toner was ~ 9 μm thick, and was smooth. The post-baked toner is impermeable to the wet etchant. Fig. 3 shows a detail of the surface profile before and after the 30-minutes post-bake at 160°C in air. The small separate peak is from an isolated toner particle.

CONCLUSION

We demonstrated a novel patterning technique for thin-film electronics, which relies on electrophotography and flexible glass foil substrates. We described the direct printing of toner on glass foil and on a-Si:H coated foil, the use of this toner as an etch mask for a-Si:H, and in the patterning of Cr by lift-off.

We wish to thank Masami Nakata and Yu Chen for depositing a-Si:H on the glass foil. This work is supported by ARPA through WPAFB under Contract F33615-94-1-4448.

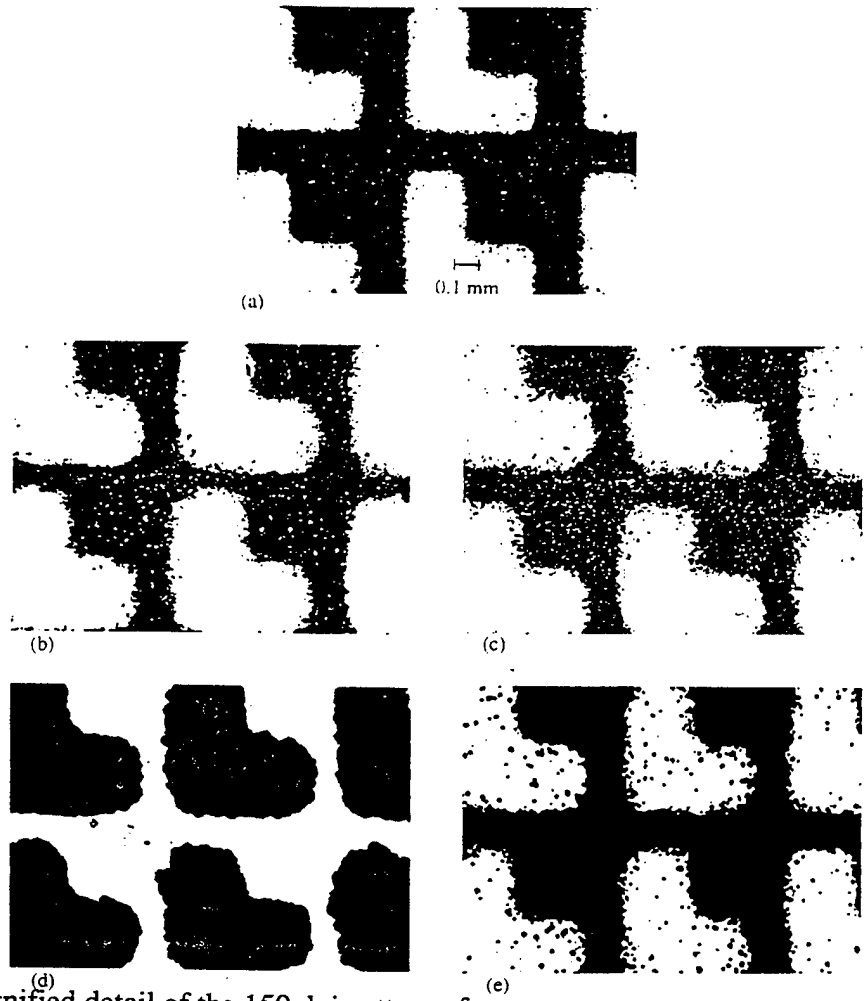

Fig. 1. Magnified detail of the 150 dpi pattern after
(a) laser-printing at 600 dpi on paper to make the original for further photocopying;
(b) photocopying on regular paper;
(c) photocopying on glass foil;
(d) patterning of a-Si:H (bright areas) by wet etch and strip;
(e) patterning of Cr (bright) by lift-off.

Fig. 2. Full view of the 8.5 in. x 11 in. glass sheet with a printed pattern.

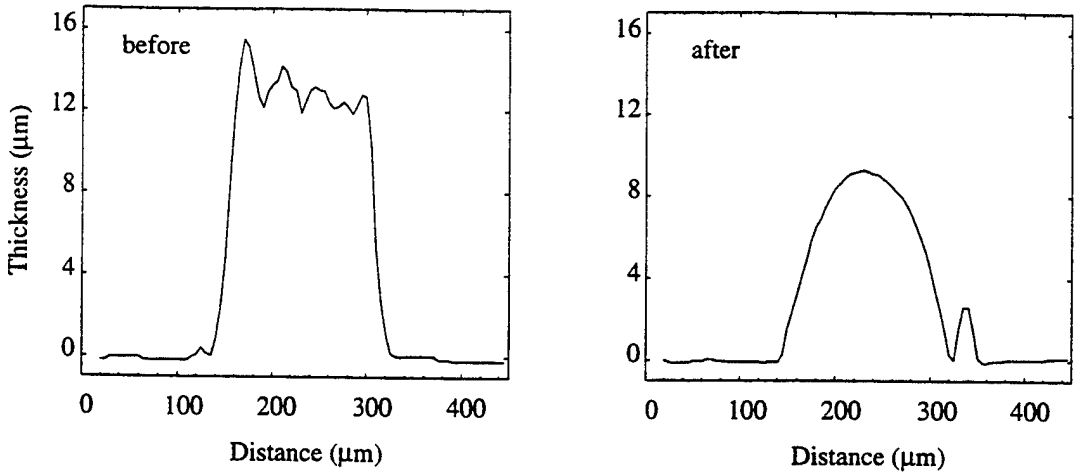

Fig. 3. Surface profile of the toner before and after post-baking at 160°C for 30 minutes. The post-bake trace shows an island made by a separate toner particle.

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Electrophotographically Patterned Thin-Film Silicon Transistors

H. Gleskova, R. Könenkamp, S. Wagner, and D. S. Shen

Abstract—**The authors made amorphous silicon thin-film transistors on glass foil using exclusively electrophotographic printing for pattern formation, contact hole opening, and device isolation. Toner masks were applied by feeding the glass substrate through a photocopier, or from laser-printed patterns on transfer paper. This all-printed patterning is an important step toward demonstrating a low-cost large-area circuit processing technology.**

I. Introduction

THE widespread introduction of large-area electronics, such as flat-panel displays, is contingent on a revolution of the manufacturing technology of integrated circuits. The cost of making a DRAM typically is \$5/cm^2. A one-square meter wall display should cost less than 10¢/cm^2. Possible sources of cost reduction are: (1) Relaxed design rules: in a square-meter size display one subpixel will measure hundreds of μm on a side; (2) Low-temperature processing technology to enable the use of a wide range of inexpensive materials; (3) Film application and patterning techniques derived form printing. In the authors' efforts to develop a large-area integrated thin-film circuit technology for consumer products, the authors are seeking to draw from these three sources.

In this letter, the authors report the fabrication of simple amorphous silicon transistors using exclusively electrophotographic printing for pattern formation, contact hole opening, and device isolation. The authors reported earlier that hydrogenated amorphous silicon (a-Si:H) can be deposited on flexible glass foil and can be patterned using an etch mask of xerographic toner. The toner was applied by feeding the a-Si:H coated glass foil through a photocopier [1]. While the performance of the transistors the authors have made to date is modest, the all-printed patterning constitutes an important step toward demonstrating a practical large-area technology.

II. Experiments

The thin-film transistors (TFT's) were fabricated on 50-μm thick alkali-free glass foil (Schott #AF45). They have a simple top gate staggered structure that requires only three patterning steps. These include direct printing [1] for the first mask level, and transfer of toner masks [2] for the higher levels. The channel length and width of the TFT's are 100 μm and 1 mm, respectively. The width of the gate electrode is 300 μm. The entire process sequence is shown in Fig. 1. The authors begin by printing the negative source-drain toner pattern, made with a laser printer, by feeding the pre-cleaned glass foil through a photocopier. This toner is baked in air at 120°C for 1 h. A 100-nm-thick layer of chromium (Cr) for the source-drain contacts then is thermally evaporated onto the substrate. The Cr is patterned by lift-off with acetone, and then the surface is cleaned further by sequential rinsing in 1,1,1-trichloroethane, acetone and methanol. The 250-nm-thick channel layer of undoped a-Si:H and the 300-nm-thick gate insulator layer of silicon nitride (SiN_x) are deposited in a three-chamber plasma enhanced chemical vapor deposition system using dc and rf excitation, respectively. An identical layer of SiN_x (not shown) then is deposited on the back side of the glass foil substrate to prevent etching of the glass by HF during further processing. Because off-the-shelf laser printers cannot register two successive layers, the authors use the transfer paper technique [2] for the second and higher mask levels. The negative gate pattern is printed on a special transfer paper using a laser printer [2]. The printed side of the transfer paper and the glass substrate are brought in contact and are aligned under an optical microscope. Applying the proper amount of heat and pressure causes the toner to stick to the substrate. Following a water soak the transfer paper is peeled off the toner. When the toner is transferred in this way, it sticks well to semiconductor and insulator layers only if they are coated with photoresist. Using the toner as a mask the photoresist is exposed to UV-light and is developed. A 100-nm-thick layer of Cr is thermally evaporated and the gate electrode is patterned by lift-off with acetone and AZ 300T stripper. In the final step, which includes source/drain contact hole opening and transistor separation, the authors again use the transfer paper technique. The authors print a positive etch mask and then etch the SiN_x in 10% HF, and the a-Si:H in KOH solution [2]. Finally, the photoresist and toner are stripped off with acetone and stripper.

III. Results and Discussion

The characteristics of a transistor fabricated as described above are shown in Fig. 2. The transistor performance reflects its simple structure and an immature process. For example, the ON current is low because the authors use direct Cr/a-Si:H instead of Cr/n^+a-Si:H/a-Si:H contacts for process sim-

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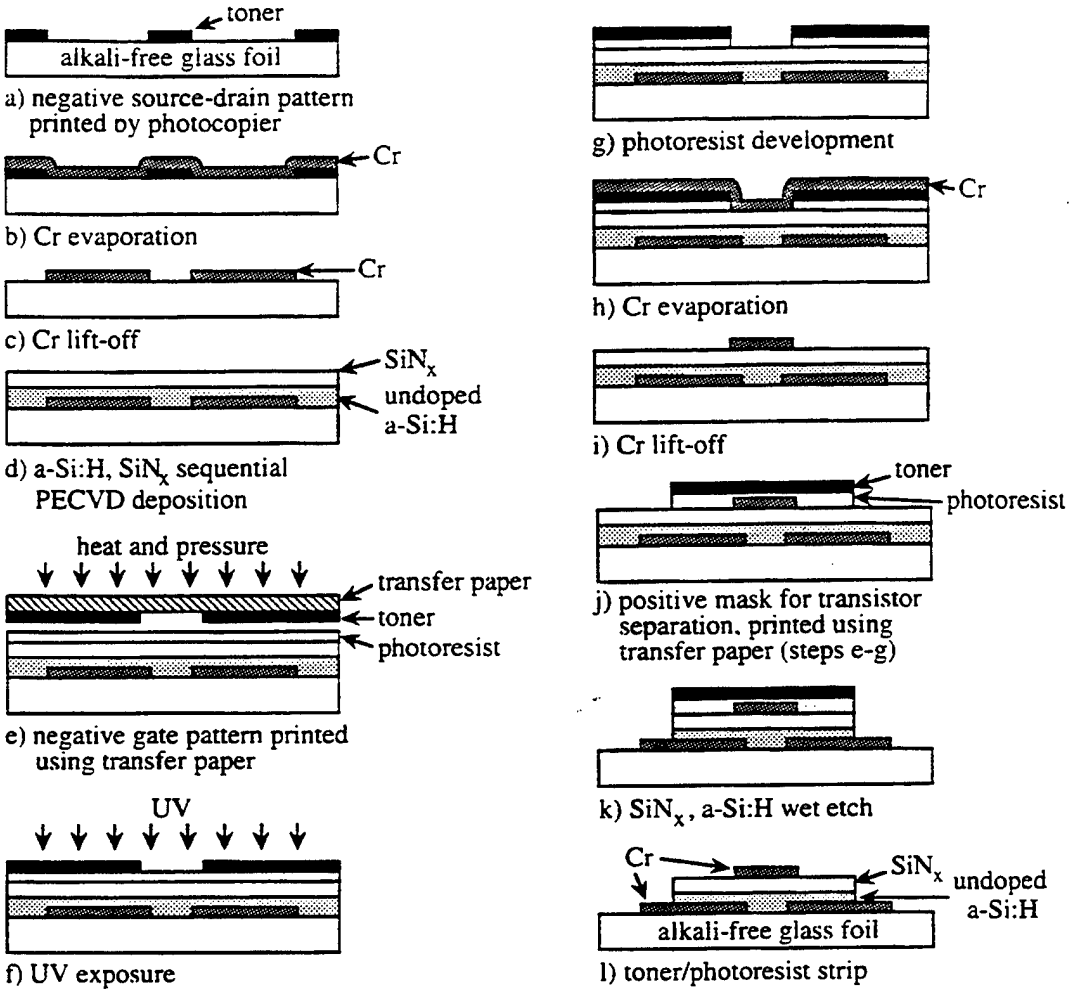

Fig. 1. TFT process sequence.

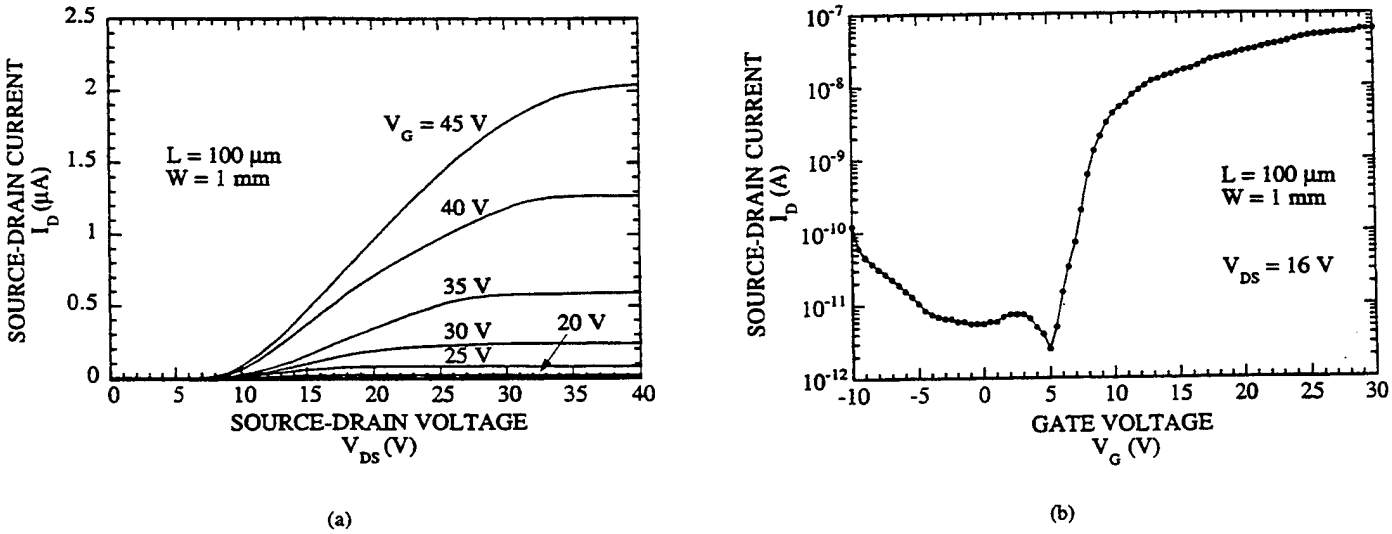

Fig. 2. Source-drain current as a function of (a) source-drain voltage for ten different gate voltages and (b) gate voltage for V_{DS} = 16 V. The source electrode is grounded.

plification. However, Fig. 2 proves that electrophotographic printing can replace all conventional photolithographic steps in TFT fabrication.

The authors' current process sequence is more complicated than the laser printing technique itself requires. This is because there is no tool available at present that allows alignment of second and higher toner levels in the laser printer. Therefore, the transfer paper technique must be relied on, which introduces into the process sequence the photoresist and associated processing steps. Alignment of each toner level with the pat-

termed substrate directly in the electrophotographic printer will eliminate the photoresist and the transfer paper steps (steps e, f, and g in Fig. 1). Such alignment tools are close to commercialization, but are not yet available in off-the-shelf printers.

Technologies exist for improving the resolution and accuracy of laser printing. In an earlier paper the authors discussed how a resolution of ~ 1 μm can be achieved when small toner particles are used in a laser printer [1]. Specialized printers using liquid toners have been developed with such resolution. Preparation of the glass surface, smaller toner particles, and thinner photoconductive layers will provide sharper edge definition and will reduce the occurrence of the errant toner particles that the authors documented earlier [2]. Consequently, adjustment of the printing process to the manufacturing needs of macroelectronics will provide a 5 μm design rule. This makes the technology suitable for large area electronics, e.g., wall-mounted displays.

Glass foil substrates enable the application of roll-to-roll printing to TFT circuit fabrication with present-day amorphous silicon technology. Using electrophotographic printing eventually will enable high throughput combined with the dynamic pattern correction needed in the manufacture of arbitrarily large-area circuits. A 5 μm design rule will enable making pixels with sizes of few 100 μm. Such pixels can be incorporated in high-definition displays with approximately 1 m (40 in) diagonals.

A number of technological improvements are needed to develop a manufacturing process. Electrophotographic printing is evolving rapidly toward meeting the requirements for the patterning of macroelectronic circuits. The authors are working on identifying a technique for aligning a higher-level toner pattern. Furthermore, as the fabrication of macroelectronic circuits is moving toward additive, printing-like processes on very large substrates, electronic techniques for pattern correction in roll-to-roll processing must be developed.

IV. Conclusion

The authors demonstrated the fabrication of amorphous silicon thin-film transistors in a process where all pattern definition steps use electrophotographic toner masks. While the process needs improvements, it already combines a drastic reduction of process steps with roll-to-roll type printing technique and electronic pattern generation. The authors view this combination as a powerful tool for developing large-area electronics.

The authors thank E. Y. Ma and S. Theiss for the help with the a-Si : H/SiN$_x$ depositions, and Schott Corporation for providing the glass foil substrates.

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a-Si:H TFT FABRICATED BY ELECTROPHOTOGRAPHIC PRINTING

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Abstract

We fabricated simple top-gate staggered amorphous silicon thin-film transistors (a-Si:H TFTs) on alkali-free glass foil using exclusively electrophotographic printing for pattern formation, contact hole opening, and device isolation. Toner masks were applied by feeding the glass substrate through a photocopier, or from laser-printed patterns on transfer paper. This all-printed patterning is an important step toward demonstrating a low-cost large-area circuit processing technology.

Introduction

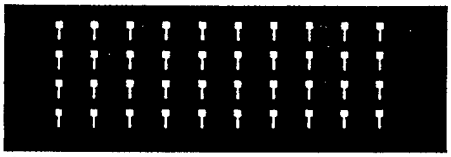
Liquid crystal display technology is pushing photolithography in the direction of very large area integrated circuits. Backplane patterning is an important contributor to LCD cost. A revolution in thin film patterning is needed to reduce this cost. Xerographic printing can cover large areas in a continuous process. Its physical limit is ~ 1 µm [1], which is satisfactory for very large displays, where pixel size may reach close to 1 mm. Therefore, we are developing electrophotographic printing to a patterning technique that reduces the number of processing steps and is fast in application.

We have demonstrated electrophotographic printing for the patterning of amorphous silicon (a-Si:H) and silicon nitride (SiN_x) deposited by plasma enhanced chemical vapor deposition (PECVD), and of thermally evaporated chromium [1,2]. The toner can be employed either as a wet etch mask, or as a shadow mask for photoresist exposure. Here we report the fabrication of simple a-Si:H TFTs using exclusively electrophotographic printing for semiconductor, gate insulator, and metal patterning, contact hole opening, and device isolation.

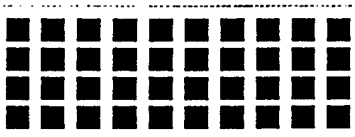
Process sequence

The TFTs were fabricated on 50-µm thick alkali-free glass foil (Schott # AF45). They have a simple top gate staggered structure that requires only three patterning steps. These include direct printing [1], and transfer [2] of toner mask. The three toner patterns are shown in Fig. 1. The channel length and width are 100 µm and 1mm, respectively. The width of the gate electrode is 300 µm. The entire process sequence is shown in Fig. 2. We begin by printing the negative source-drain toner pattern (made with a laser printer, see Fig. 1a) by feeding the pre-cleaned glass foil through a photocopier. This toner is baked in air at 120°C for one hour. Then a 100-nm-thick layer of chromium (Cr) for the source-drain contacts is thermally evaporated onto the substrate. The Cr is patterned by lift-off with acetone, and the surface is cleaned further by sequential rinsing in 1,1,1-trichloroethane, acetone and methanol. The 250 nm thick channel layer of undoped a-Si:H and the 300 nm thick gate insulator layer of silicon nitride (SiN_x) are deposited in a three-chamber PECVD system using dc and rf excitation, respectively. An identical layer of SiN_x then is deposited on the back side of the glass foil substrate (not shown) to passivate the glass against HF etching during further processing. For the following patterning steps we use the transfer paper technique [2] to enable alignment between mask levels. The negative gate pattern (Fig. 1b) is printed on a special transfer paper using a laser printer. The printed side of the transfer paper and the glass substrate are brought in contact and are aligned under an optical microscope. Applying the proper amount of heat and pressure causes the toner to stick to the substrate. The transfer paper is peeled off the toner after a water soak. Semiconductor and insulator layers must be coated with photoresist before toner transfer. Following toner transfer, the sample is exposed to UV-light (using the toner as a shadow mask) and the photoresist is developed. A 100-nm-thick layer of Cr is thermally evaporated and the gate electrode is patterned by lift-off with acetone and AZ 300T stripper. For the final step, which includes source/drain contact hole opening and transistor separation, we again use the transfer paper technique. We print a positive etch mask (Fig. 1c) and then etch the SiN_x in 10% HF, and the a-Si:H in KOH solution at 50°C [2]. Finally, the photoresist and toner are stripped off with acetone.

a) Negative source-drain pattern.



b) Negative gate pattern.



c) Positive pattern for contact hole opening and transistor separation.

Figure 1. Toner masks used for the patterning steps.

Results and discussion

The characteristics of a transistor fabricated as described above are shown in Fig. 3. Fig. 3(a) shows the source-drain current as a function of source-drain voltage for ten different

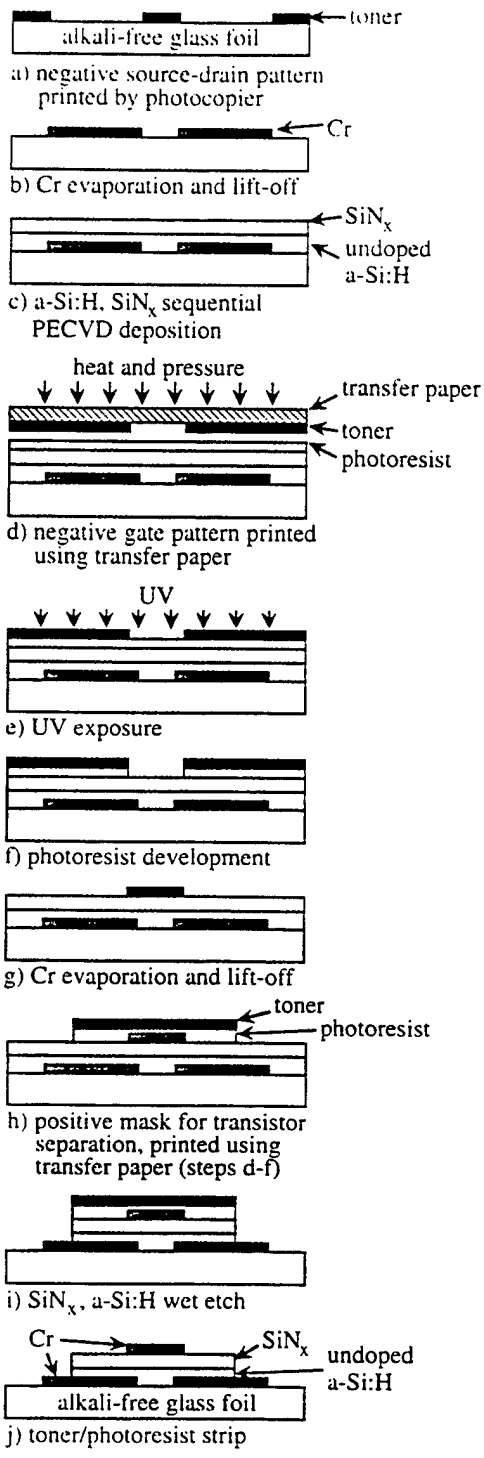


Figure 2. Process sequence.

gate voltages ranging from 0 to 45 V. The source-drain current as a function of gate voltage is shown in Fig. 3(b). While the transistor performance reflects its simple structure and an immature process, Fig. 3 proves that electrophotographic printing can replace all conventional photolithographic steps in TFT fabrication.

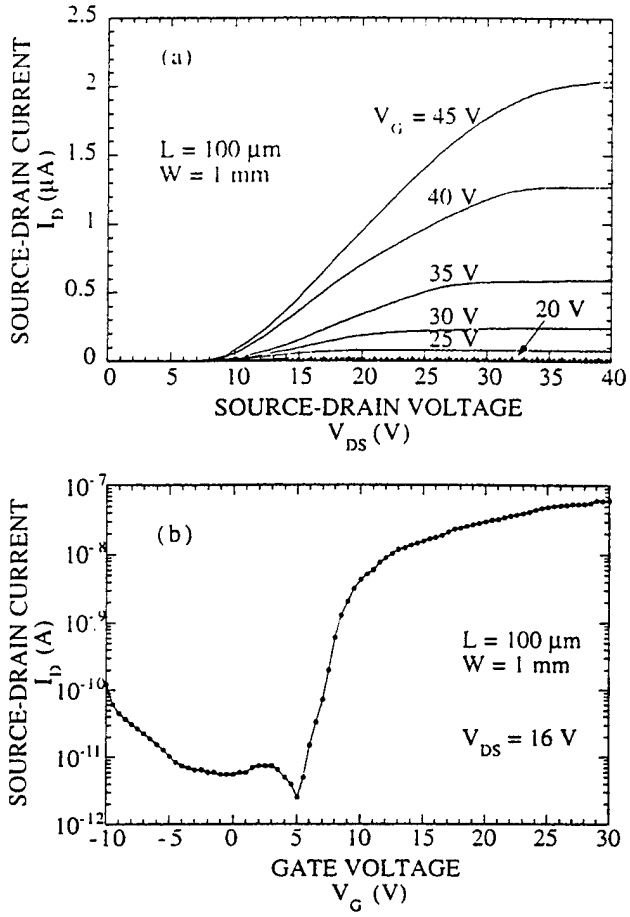


Figure 3. Transistor characteristics. a) Source-drain current as a function of source-drain voltage for ten different gate voltages. b) Source-drain current as a function of gate voltage for V_{DS} = 16 V.

Summary

We demonstrated the fabrication of a-Si:H TFTs in a process where all pattern definition steps use electrophotographic toner masks. While the process needs improvements, it already combines a drastic reduction of process steps using printing technique and electronic pattern generation. We view this combination as a powerful tool for developing large-area electronics.

This work is supported by ARPA through WPAFB under Contract F33615-94-1-4448. We thank R. Könenkamp and S. Theiss for the help with the a-Si:H/SiN_x depositions, and Schott Corporation for providing the glass foil substrates.

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* On leave from the Department of Solid State Physics, Comenius University, 84215 Bratislava, Slovakia.

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2. H. Gleskova, S. Wagner and D.S. Shen, "Electrophotographic Patterning of a-Si:H", Materials Research Soc. Symp. Proc. 377 (1995) - to be published.

HR5' 96

a-Si:H TFTs PATTERNED USING LASER-PRINTED TONER

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ABSTRACT

We fabricated top-gate amorphous silicon thin-film transistors (a-Si:H TFTs) on alkali-free glass foil, for the first time using laser-printed toner for the patterning of each layer. The toner for the first mask level was applied by feeding the glass foil through a laser printer, and for the following mask levels from patterns laser-printed on transfer paper. The transistors have off currents from ~ 10^{-12} A to ~ 10^{-11} A and on-off current ratios of ~ 10^6. Thus we have demonstrated a technology for the patterning of TFT circuits by printing.

INTRODUCTION

The flat-panel display industry introduced a new trend in semiconductor technology -- scaling-up replaced miniaturization. The semiconductor processing tools developed for integrated circuit fabrication were scaled up to accommodate the size of the active matrix. Newly developed mass-production sputtering and dry-etching systems [1] and also steppers can handle substrates up to 40 x 50 cm^2, but they are correspondingly expensive. We need a revolution of the manufacturing technology of integrated circuits to reduce the cost of future wall-size displays. In our effort to develop a large-area integrated thin-film circuit technology for such consumer products, we have replaced photolithography with electrophotographic printing. Electrophotography, a mature technique used in laser printers and photocopiers, already allows to print with a resolution of 1800-2400 dpi, leading to a design rule of 11-15 μm, with further reduction in sight [2]. Commercial large-area photocopiers handle three-feet wide rolls of paper. Combining a laser printer with a computer offers a simple means for the generation of toner masks and their dynamic correction. The toner masks can be directly applied to semiconductor, insulator, and metal surfaces [2] without any further patterning.

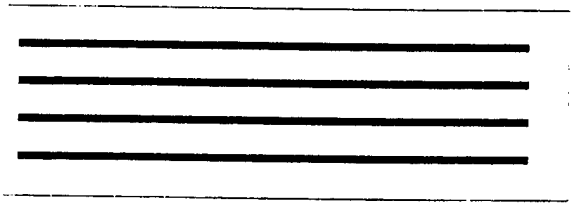
We reported earlier that hydrogenated amorphous silicon (a-Si:H) can be deposited on flexible glass foil and can be patterned using an etch mask of xerographic toner [2]. Recently, we have shown that a-Si:H TFTs can be made by using toner masks for the patterning of all layers [3]. In this paper we report improved electrophotographic processing that provides TFTs with improved electrical performance.

EXPERIMENTAL PROCEDURES

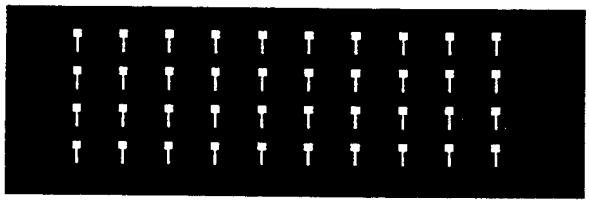
TFTs were fabricated on 50-μm thick alkali-free glass foil (Schott # AF45). The TFTs have a top-gate staggered structure that requires three different patterning steps. These include direct laser printing [2] for the first mask level, and transfer of toner masks [4] for the higher levels. The three toner patterns are shown in Fig. 1.

The channel length and width of the TFTs are 100 μm and 1mm, respectively. The width of the gate electrode is 250 μm. The entire process sequence is shown in Fig. 2. First, a ~ 100 nm thick Cr layer is thermally evaporated over the clean glass substrate. Then a ~ 100 nm thick (n^+) a-Si:H layer is deposited on the Cr using rf plasma enhanced chemical vapor deposition (PECVD). The positive source-drain toner pattern (see Fig. 1a) is printed on the (n^+) a-Si:H layer by feeding the glass foil through a commercial 600 dpi laser printer. After printing, the toner is further baked at 120°C for 1 hour in air. During this additional baking the sintered toner clusters fuse together and create a continuous layer of polymer toner. Using this mask, the (n^+) a-Si:H layer is etched in KOH solution [2]. Then the toner is stripped in an ultrasonic bath of PRX 100 stripper [5] heated to 80°C. The Cr layer is etched in CAN etch [6] at room temperature. In this case the patterned (n^+) a-Si:H layer serves as a mask. The 170-nm-thick channel layer of undoped a-Si:H and the 300-nm-thick gate insulator layer of silicon nitride (SiN_x) are deposited in a three-chamber PECVD system using rf excitation.

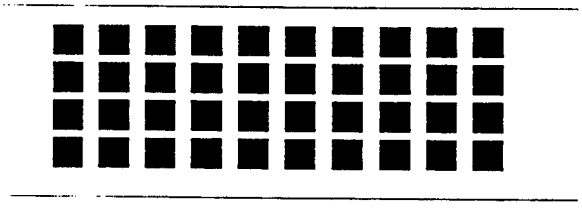
Because with our off-the-shelf laser printers we cannot register two successive layers, we use the transfer paper technique [4] for the second and higher mask levels. The negative gate pattern (see Fig. 1b) is printed on a special transfer paper using the above mentioned laser printer. The printed side of the transfer paper and the glass substrate are brought in contact and are aligned under an optical microscope. Applying the proper amount of heat and normal force causes the toner to stick to the substrate. Following a water soak the transfer paper is peeled off the toner. Unfortunately, when the toner is transferred in this way, it sticks well to semiconductor and insulator layers only if they are coated with photoresist. Using the toner as a UV-mask the photoresist is exposed to UV-light and is developed. A ~ 100-nm-thick layer of Al is thermally



(a) Positive source-drain mask.



(b) Negative gate mask.



(c) Positive mask for contact hole opening and transistor separation.

Fig. 1. Toner masks for TFT fabrication.

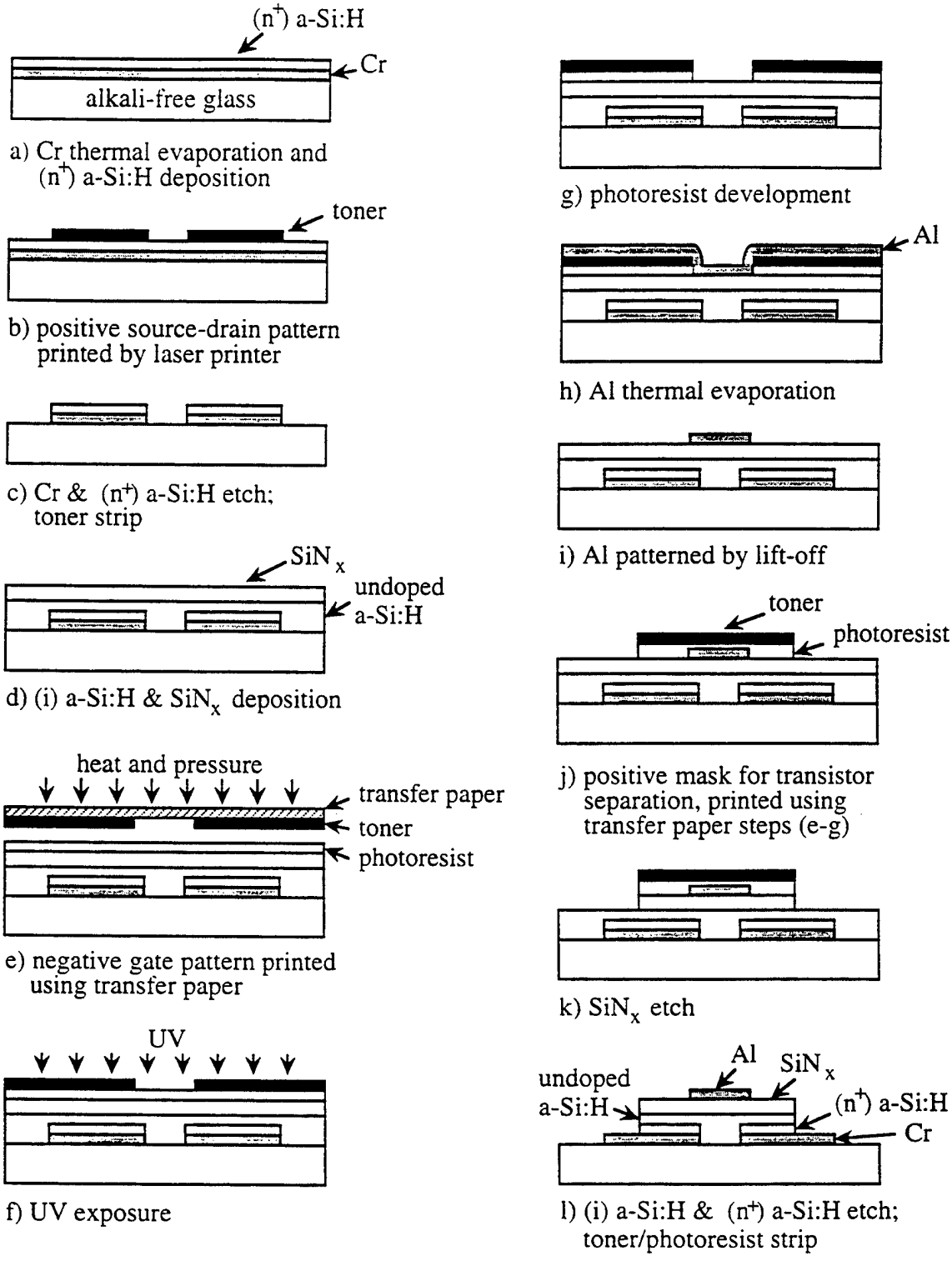


Fig. 2. TFT process sequence.

evaporated and the gate electrode is patterned by lift-off with PRX 100 stripper. In the final step, which includes source/drain contact hole opening and transistor separation, we again use the transfer paper technique. We print a positive etch mask (see Fig. 1c) and then etch the SiN_x in 10% HF. The undoped and (n^+) a-Si:H are etched in AZ 300 T stripper heated to ~ 130°C which simultaneously strips the toner/photoresist layer.

RESULTS AND DISCUSSION

The characteristics of a transistor fabricated as described above are shown in Fig. 3. Fig. 3(a) shows the dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for V = 10 V. The off-current is 1 x 10^{-12} A and the ratio of the on-off current is ~ 10^6. The transistors have a relatively high threshold voltage which is also visible in Fig. 3(b). This figure shows the source-drain current as a function of source-drain voltage V_{ds} for eight different gate voltages ranging from 0 to 45 V. A magnified photograph of that particular transistor is shown in Fig. 4.

In the saturation regime the source-drain current is given by:

$$I_{ds} = (W/2L)\, C_{SiN}\, \mu_n\, (V_{gs} - V_t)^2$$

where L is the channel length, W the channel width, C_{SiN} the capacitance of the gate insulator, μ_n the electron mobility, and V_t the threshold voltage. Plotting $(I_{ds})^{1/2}$ versus V_{gs} gives a value of ~ 12 V for the threshold voltage and a value of 8.32 x 10^{-9} F V^{-1} s^{-1} for the (C_{SiN} μ_n) product. Because $C_{SiN} = \varepsilon_o\, \varepsilon_r / d_{SiN}$, a value of 2.07 x 10^{-8} F cm^{-2} is calculated for the capacitance of the nitride, assuming ε_r = 7. The corresponding calculated mobility is 0.40 cm^2 V^{-1} s^{-1}. This a reasonable value given our immature technology. On the same glass substrate we also fabricated transistors from which the (n^+) a-Si:H layer was removed on purpose. Their characteristics look very similar to those of TFTs with the (n^+) a-Si:H layer. This suggests that the n^+ layer does not affect the contact between the Cr source-drain metallization and the undoped a-Si:H, probably because of the relatively low saturation current densities.

Our current process sequence is more complicated than the laser printing technique itself requires. This is because we have no tool available at present that allows us to align second and higher toner levels in the laser printer. Therefore, we need to rely on the transfer paper technique, which introduces to the process sequence the photoresist and associated processing steps. Alignment of each toner level with the patterned substrate directly in the electrophotographic printer will eliminate the photoresist and the transfer paper steps (steps e, f, and g in Fig. 2). Such alignment tools are close to commercialization, but are not yet available in off-the-shelf printers.

SUMMARY

We fabricated amorphous silicon thin-film transistors for the first time in a process where all pattern definition steps use electrophotographic toner masks. While the process needs improvements, it already combines the potential for a drastic reduction of process steps with the advantage of electronic pattern generation. We view this combination as a powerful tool for developing large-area electronics.

This work is supported by ARPA through WPAFB under Contract F33615-94-1-4448 and by EPRI. We thank S. D. Theiss for the help with the SiN_x depositions, and Schott Corporation for providing the glass foil substrates.

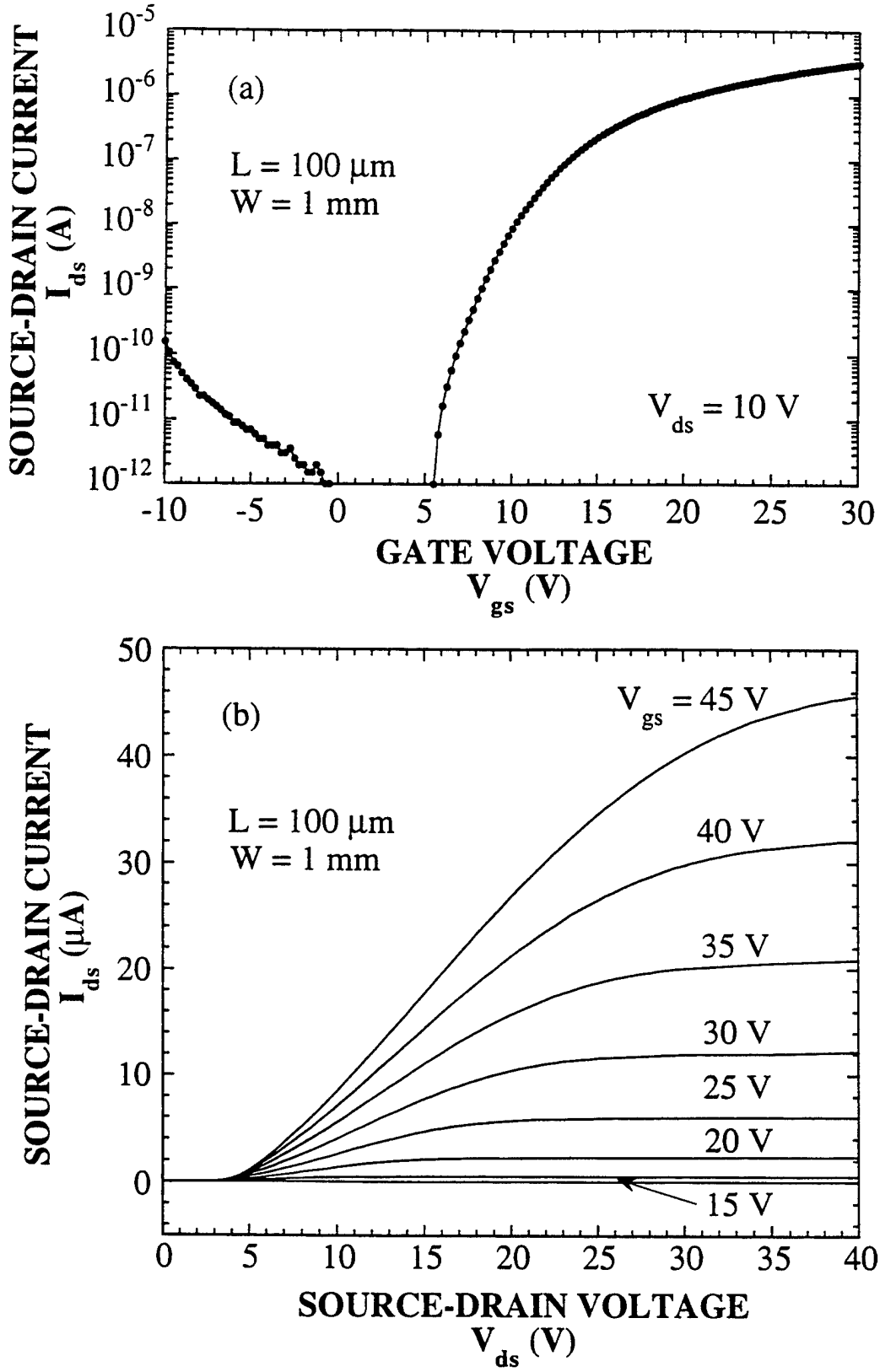


Fig. 3. Source-drain current as a function of a) gate voltage for V_{ds} = 10 V, b) source-drain voltage for eight different gate voltages. The source electrode is grounded.

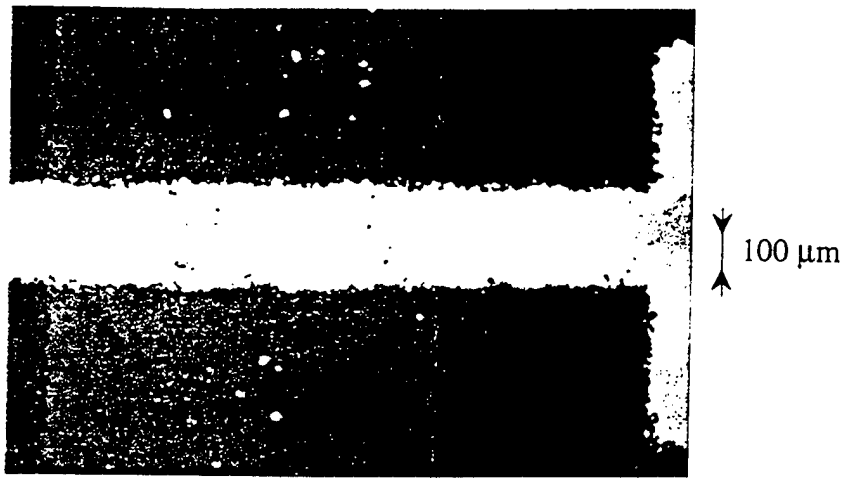


Fig. 4. Magnified photograph of the transistor whose characteristics are shown in Fig. 3.

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6. Foto Chemical Systems, Inc., Wayne, NJ 07474-3188.

JAN '97

PHOTORESIST-FREE FABRICATION PROCESS FOR a-Si:H TFTs

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We fabricated a-Si:H thin-film transistors by using only computer-generated masks of xerographic toner, which replaces photoresist in each patterning step. This photoresist-free process produces high quality TFTs with an on/off current ratio of ~ 10^7, a threshold voltage of ~ 3 V and an electron mobility of ~ 1 $cm^2 V^{-1} s^{-1}$.

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Introduction.

Large-area electronics, or macroelectronics, is the most important application of amorphous silicon, with active matrix backplanes for liquid crystal displays being most prominent at present. The manufacturing cost of a-Si:H macroelectronics must be reduced to expand its use. We have been demonstrating that a great potential for cost reduction is opened when xerographically printed toner masks are substituted for photoresist [1,2]. By using printed toner instead of photoresist masks, we eliminate three process steps from each mask level (Fig. 1). In this paper we show that entire thin-film transistors (TFTs) can be made by using only toner masks.

Experiments.

We fabricated an array of a-Si:H TFTs on 50-μm thick alkali-free glass foil (Schott # AF45), with the glass foil providing the flexibility required by our off-the-shelf laser printer. Our bottom-gate, back-channel-etch TFTs need four patterning steps ("mask levels"). These steps include direct laser printing [1] for the first mask level, and toner transfer [2] for the higher levels. We use the transfer paper technique [2] for the higher levels, because with our laser printer we cannot register two successive levels. The four toner patterns are written by Postscript and are shown in Fig. 2.

The channel length L and width W of the TFTs are 100 μm and 500 μm, respectively. The gate electrode is 300 μm long. The entire process sequence is shown in Fig. 3. First, we print a negative toner gate mask by running the glass foil through the laser printer. Then an ~ 100 nm thick Cr layer is thermally evaporated and the Cr/toner is lifted-off in toluene. We deposit a sequence of the following layers in a three-chamber plasma enhanced chemical vapor deposition system: ~ 410 nm of SiN_x, ~ 160 nm of undoped a-Si:H, and ~ 50 nm of (n^+) a-Si:H. An ~ 100 nm thick Cr layer is thermally evaporated. We print a positive source-drain

toner pattern using transfer paper. Then the Cr layer is wet etched, the toner removed, and the (n^+) a-Si:H layer dry etched in CF_4. Next, we print a positive toner mask for the TFT island formation, again using transfer paper. The undoped a-Si:H layer is dry etched in CF_4. Without stripping the mask, we print the final toner mask for the gate electrode opening, again using transfer paper. The SiN_x is dry etched in CF_4 and the toner removed. Because the nitride is etched only in the areas of the gate electrode pad it is not visible in Fig. 3(i). Finally, the TFTs are annealed for 30 min. in forming gas at 200°C to anneal out the radiation damage caused by the plasma during dry etching.

Results and discussion.

The characteristics of a transistor fabricated as described above are shown in Fig. 4. This figure shows the dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for V_{ds} = 0.1 V or 10 V. The off-current is ~ 2 x 10^{-12} A and the on/off current ratio is ~ 10^7. In the linear approximation the source-drain current is given by:

$$I_{ds} = \frac{W}{L} C_{SiN} \mu_n \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

where L is the channel length, W the channel width, C_{SiN} the capacitance of the gate insulator, μ_n the electron mobility, and V_T the threshold voltage. At V_{ds} = 0.1 V we obtain V_T ~ 3 V and a value 7.7 x 10^{-9} A V^{-1} for the (C_{SiN} μ_n V_{ds} W / L) product. Using ε_{SiN} = 7.0 we calculate an electron mobility of ~ 1 cm^2 V^{-1} s^{-1}. Thus we have made a-Si:H TFTs with electrical performance comparable to that of a-Si:H TFTs fabricated using conventional photolithography.

Typical toners are based on polystyrene or polyethylene. After printing we usually post-bake to fuse the toner into a layer that is impermeable to liquid etchants. The toner replaces photoresist in all its functions, i.e., as a wet or dry etch mask or as a mask for lift-off. The

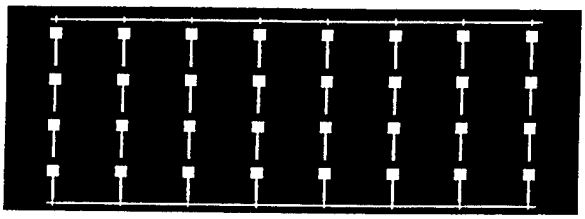
toner can be removed with commercial photoresist strippers or in unblended organic solvents. As shown in Fig. 3(h) several toner masks may be printed on top of each other, which further reduces the number of process steps and thus simplifies manufacturing.

The 100-μm channel length of our TFTs is chosen to conform with the resolution of our 600 dpi laser printer (~ 40 μm design rule). The roughness of the pattern edges (see Fig. 4) is of the order of 10 μm and is determined by the typical particle size of a dry toner. Liquid toners, which are dispersions of toner particles in low-polarity liquids, use toner sizes down to 1 μm. The diffraction limit of laser writing lies below 1 μm. With the diameter of the toner particles reduced from 10 μm to 1 μm, i.e., by a factor of 10, the mass of the particles is reduced by a factor of 1000. Therefore, the surface of the photoconductive layer of the laser printer can be charged to a much lower voltage to hold the toner particles. This allows to reduce the thickness of the photoconductor from the typical value of ~ 20 μm to close to 1 μm, which increases the lateral resolution of the electrostatic pattern written in the photoconductor surface. The preceding consideration of toner size, laser resolution and photoconductor thickness all suggest that electrophotographic printing with 1 μm design rule is feasible.

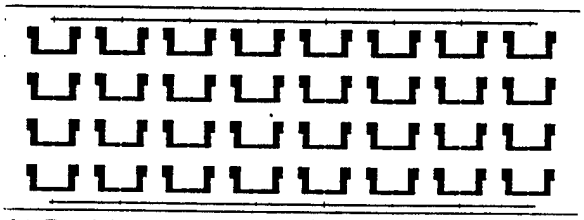
Computer generation of the mask pattern opens the prospect of real-time pattern correction, which will become a necessity in high-speed printing. The preceding pattern will be read by a scanner, and will be compared with the computer-stored pattern of the next mask level. The stored pattern then can be adjusted, to enable the direct printing of a real-time-corrected overlay.

Conclusion.

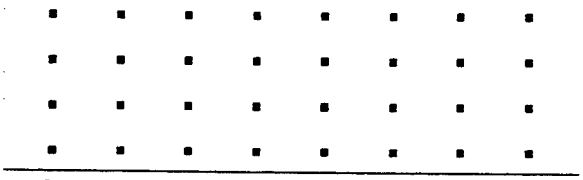
We fabricated bottom-gate back-channel etch amorphous silicon thin-film transistors by a process where all four pattern definition steps use electrophotographic toner masks. This process combines the potential for a drastic reduction of process steps with the advantage of electronic pattern generation, and provides high-quality TFTs.



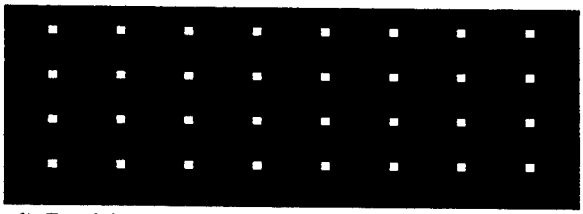
a) Negative gate mask



b) Positive source-drain mask



c) Positive mask for TFT island

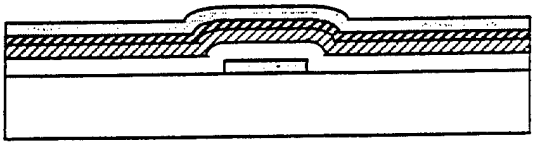


d) Positive mask for gate electrode opening

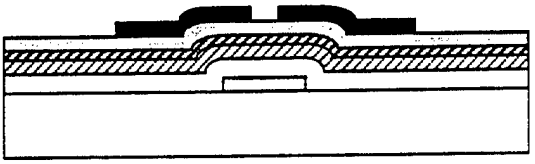
Cross-section through the transistor island

a) Negative toner gate pattern, printed using laser printer

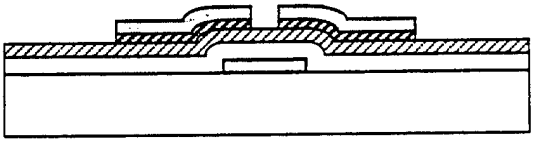
b) Cr thermal evaporation and lift-off



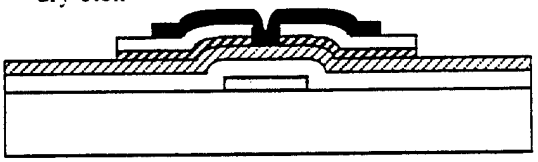
c) SiN_x, a-Si:H and (n+) a-Si:H deposition: Cr thermal evaporation



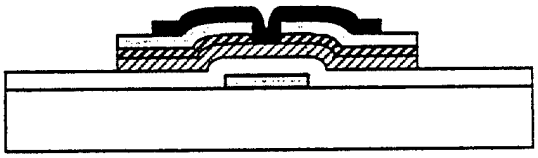
d) Positive toner source-drain mask, printed using transfer paper



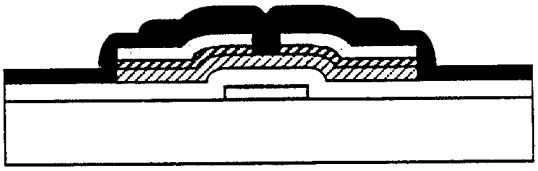
e) Cr wet etch, toner removal and (n^+) a-Si:H dry etch



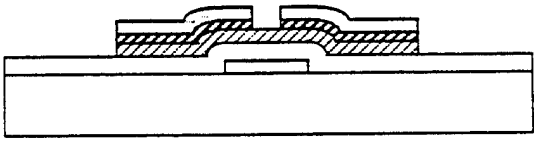
f) Positive toner mask for transistor island, printed using transfer paper



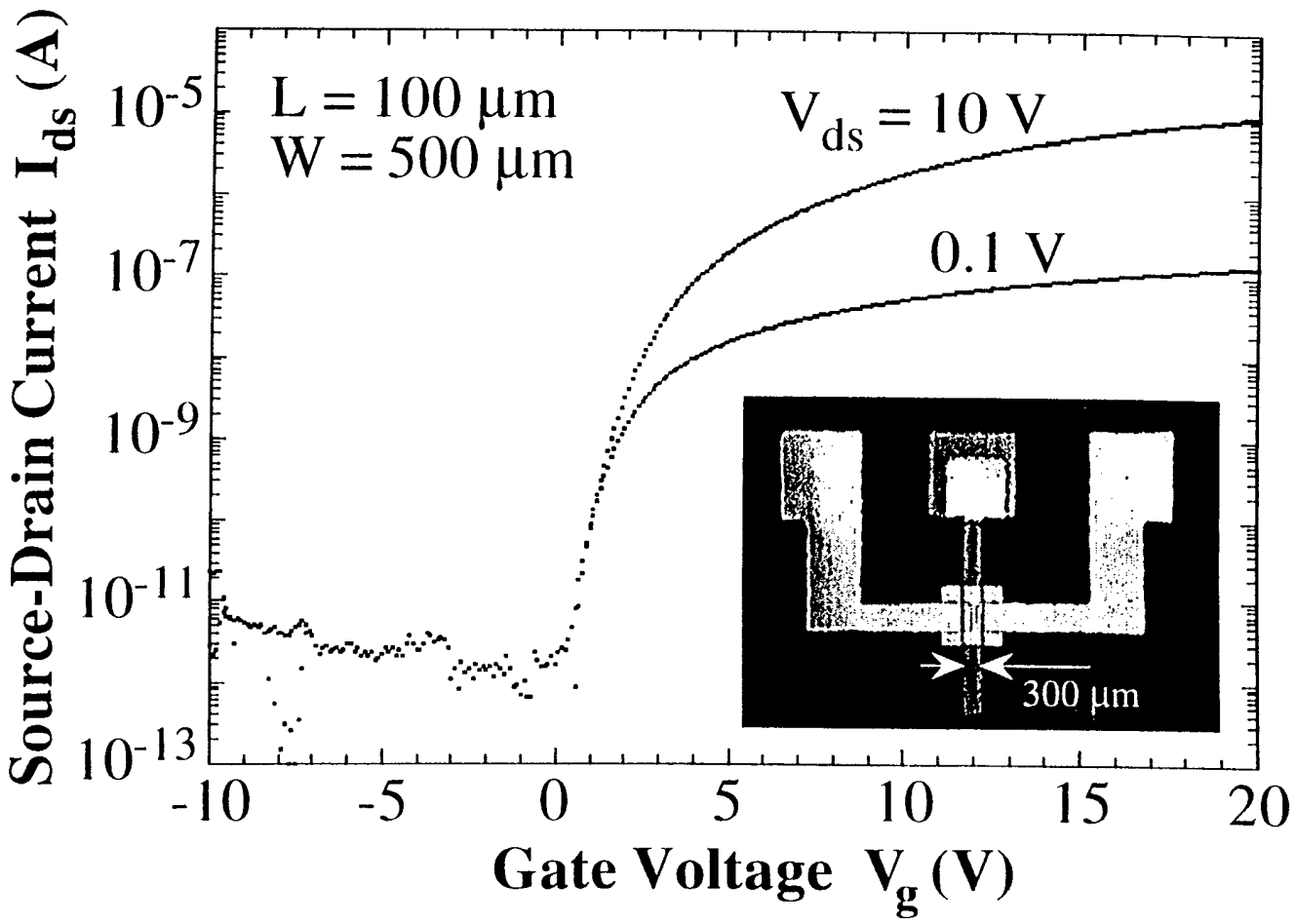
g) (i) a-Si:H dry etch



h) Positive mask for gate electrode opening, printed using transfer paper



i) SiN_x dry etch, toner removal


L = 100 µm
W = 500 µm
V_{ds} = 10 V
0.1 V
300 µm
Source-Drain Current I_{ds} (A)
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
-10
-5
0
5
10
15
20
Gate Voltage V_g (V)

This work is supported by DARPA through WPAFB under Contract F33615-94-1-4448, and by EPRI. We thank Schott Corporation for providing the glass foil substrates.

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2. H. Gleskova, S. Wagner and D.S. Shen, Mat. Res. Soc. Symp. Proc. **467** (1997) - to be published.

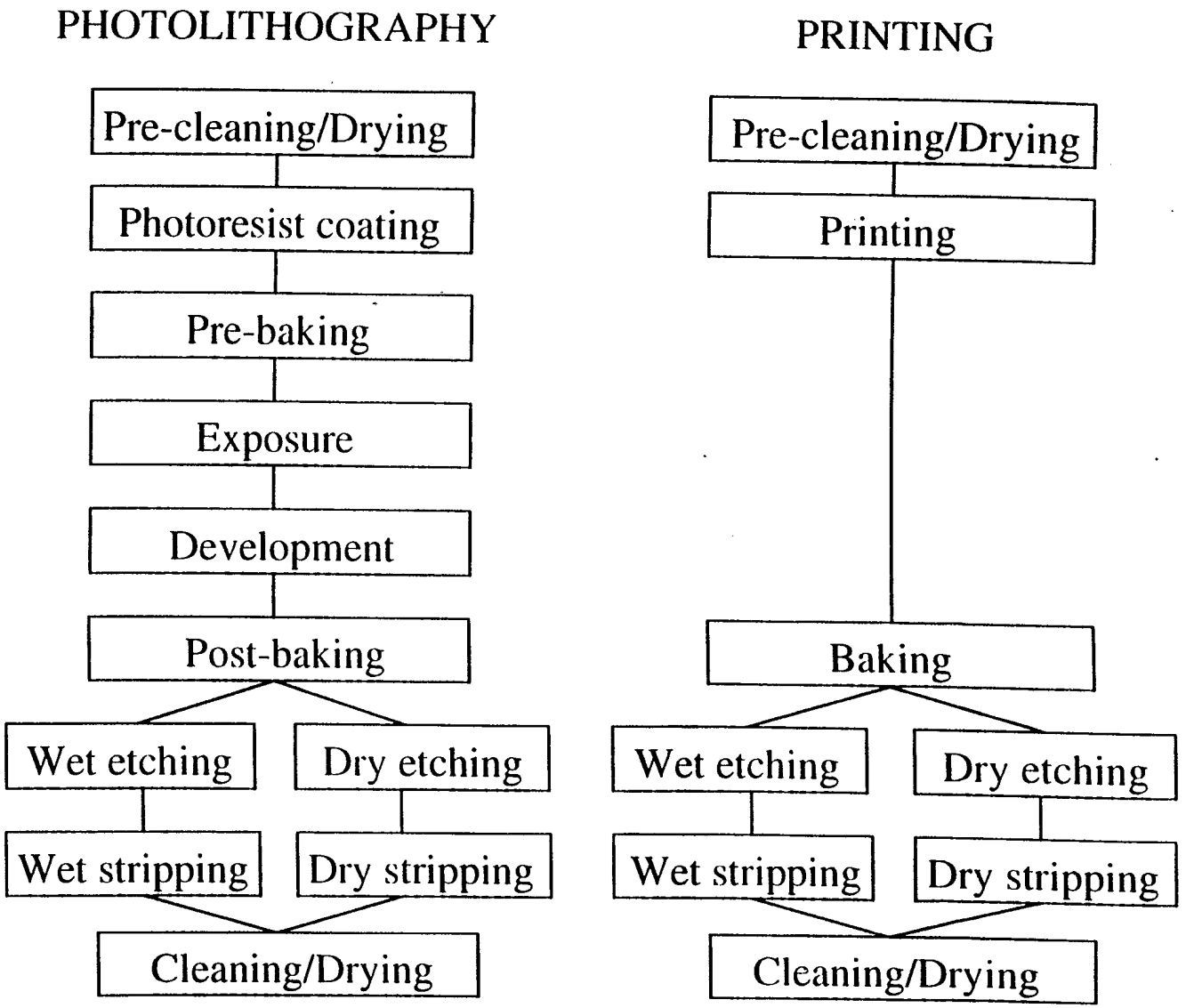
Figure captions.

Fig. 1. Comparison of the process steps for photoresist and toner masks.

Fig. 2. Toner masks for TFT fabrication.

Fig. 3. TFT process sequence.

Fig. 4. TFT characteristics. The source electrode is grounded. The insert is a photograph of a TFT, including the contact pads.


PHOTOLITHOGRAPHY
Pre-cleaning/Drying
Photoresist coating
Pre-baking
Exposure
Development
Post-baking
Wet etching
Dry etching
Wet stripping
Dry stripping
Cleaning/Drying
PRINTING
Pre-cleaning/Drying
Printing
Baking
Wet etching
Dry etching
Wet stripping
Dry stripping
Cleaning/Drying

Flexible Glass Substrates with Via Holes for TFT Backplanes.

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We demonstrate a new technology for RC gate delay reduction, by fabricating an array of amorphous silicon thin-film transistors (a-Si:H TFTs) on a thin glass substrate with via holes. All gates are connected through via holes to a metal line that is run on the bottom of the substrate. We opened via holes with a diameter of 30 to 40 μm in 50 μm glass foil, and use a process which employs electrophotographic toner masks for all pattern definition steps.

1. Introduction

Dramatic technology and productivity improvements for TFT backplanes are possible when thin, flexible substrates are used. We have shown that high-performance TFTs can be made on 30 to 80 μm thick glass foil substrates by printing xerographic toner at all mask levels [1, 2].

Here we show that the size restriction on a display that results from the RC time constant for the bottom metal line can be relaxed. In a-Si:H TFTs the bottom metal usually is the gate. We open via holes through the substrate, and connect the TFT gates on the top side with a gate line that is run on the bottom. Because this line is not part of the semiconductor structure, it can be made much thicker than on the front. As a result, the gate RC delay can be reduced greatly.

Fig. 1 shows a simple model of display line resistance. In figure 1a a line with resistance R is driven from a source on the left side. Figure 1b shows that if a perfect conductor is added on the bottom side of the glass and linked to the top metal at the edges of the plate, the highest resistance R_{max}, to the center of the line, is R/4. In fact, this is equivalent to driving the line from both the left and the right ends. In the following discussion we will concentrate on driving from only one side. For a non-ideal bottom line of total resistance of R/n (Figure 1c), it can be shown that R_{max} and its position x_{max} are as follows:

$$R_{max} = \frac{R}{4}\left(1 + \frac{1}{n}\right), \quad x_{max} = \frac{1}{2}\left(1 + \frac{1}{n}\right)$$

It is clear that when n becomes large (perfect conductor or line driven from both ends), R_{max} approaches R/4, and the point of highest resistance is shifted to the center.

If via holes are added along the line and contacts are made through the holes, the highest resistance R_{max} is located in the section farthest from the source, and is given by:

$$R_{max} = \frac{R\,(m\text{-}1)}{m\,(1+n)} + \frac{R}{4m}\left(1 + \frac{1}{n}\right)$$

Here m is the number of line segments, and (m+1) is the number of top-to-bottom connections.

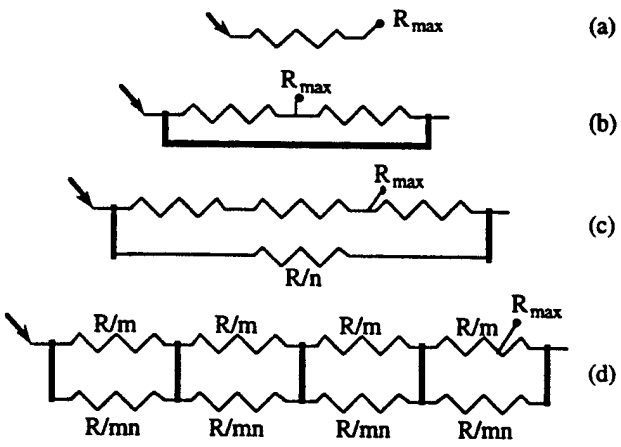


Figure 1. Simple equivalent circuit of top and bottom gate conductors with via hole connections (vertical bars), (a) line driven from one side, (b) connection at both plate edges to a perfect conductor on the bottom, (c) same as (b) but non-perfect bottom conductor, (d) general case.

Fig. 2 shows R_{max}/R as a function of n, using m as parameter. Two points are clear from the figure. First, when the resistance of the bottom line is reduced, the resistance drops rapidly first, and then saturates near n=10: when the bottom resistance becomes one order of magnitude lower than the resistance of top line, reducing it further has no perceptible effect. Second, not many via

holes are needed to further reduce the resistance. Five via holes (m=4) with a thick bottom line (e.g. n=5) bring the maximum resistance down to ~ 20% of the top-line-only value. Conversely, this particular configuration would allow increasing the panel size by a factor of 5.

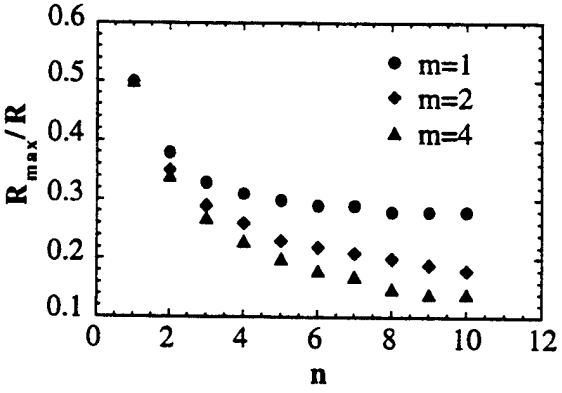


Figure 2. Effect of the bottom wire resistance R/n and of the number m of via holes on the normalized maximum resistance.

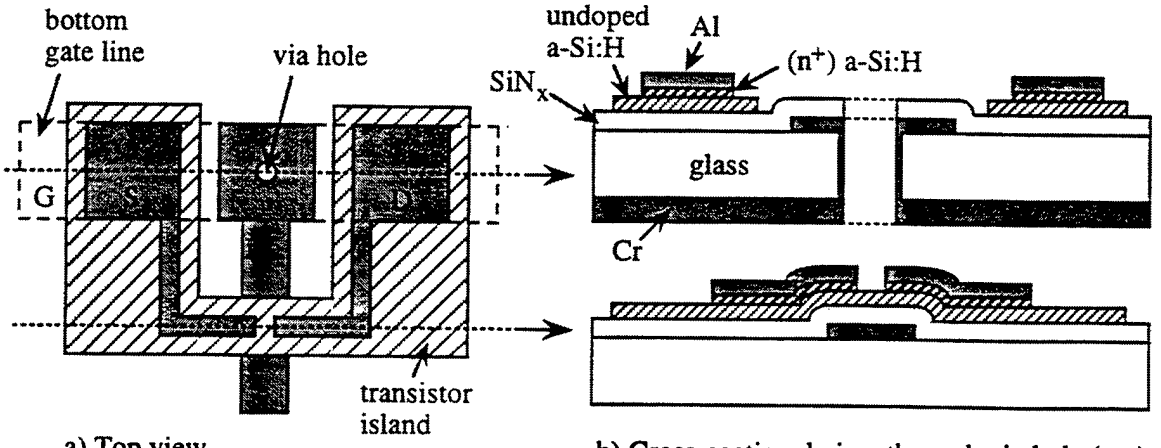
2. Experiments

The via holes were fabricated in a 50 μm glass foil (Schott # AF 45). We tested three different techniques: wet etching, ultrasonic drilling and laser drilling. The laser drilling provided the smallest holes, of 30 to 40 μm diameter.

The TFTs have a bottom gate, back-channel etch structure. Our simple process requires only three different patterning steps. Each patterning step uses a mask of laser printed toner [1,2]. Each gate conductor pad of the TFT is collocated with a via hole, and each gate is connected through this via hole to the Cr line run on the bottom side of the substrate. A 3 x 1.5 $inch^2$ glass substrate with 32 via holes was used. A top and two cross-sectional views of the TFT structure are shown in Fig. 3. The schematic process sequence is shown in Fig. 4.

First, we printed a negative toner gate mask on a glass substrate using transfer paper [2]. The transfer paper procedure is very similar to the one published before [2] except now we do not use photoresist as adhesion layer. Then a ~ 100 nm thick Cr layer was thermally evaporated and the toner was lifted-off in PRX 100 stripper. The bottom ~ 200 nm thick Cr lines, connecting the gates horizontally, were thermally evaporated through a metal mask.

After the top-to-bottom Cr connections were fabricated, we deposited a sequence of the following layers in a multi-chamber deposition system: ~ 450 nm of SiN_x, ~ 250 nm of undoped a-Si:H, and ~ 50 nm of (n^+) a-Si:H. An ~ 100 nm thick Al layer was thermally evaporated. We printed a positive source-drain toner pattern using transfer paper [2]. Then the Al layer was wet etched, the toner was stripped-off, and the (n^+) a-Si:H layer was dry etched in CF_4 gas. Next, we printed a positive toner mask for transistor separation, again using the transfer paper. The undoped a-Si:H layer was etched in KOH solution, and the toner was stripped off. Finally, we dry-etched the substrate from the bottom to remove any SiN_x from the holes.



a) Top view

b) Cross-sectional view through via hole (top) and through TFT (bottom).

Figure 3. Top and cross-sectional views of one TFT

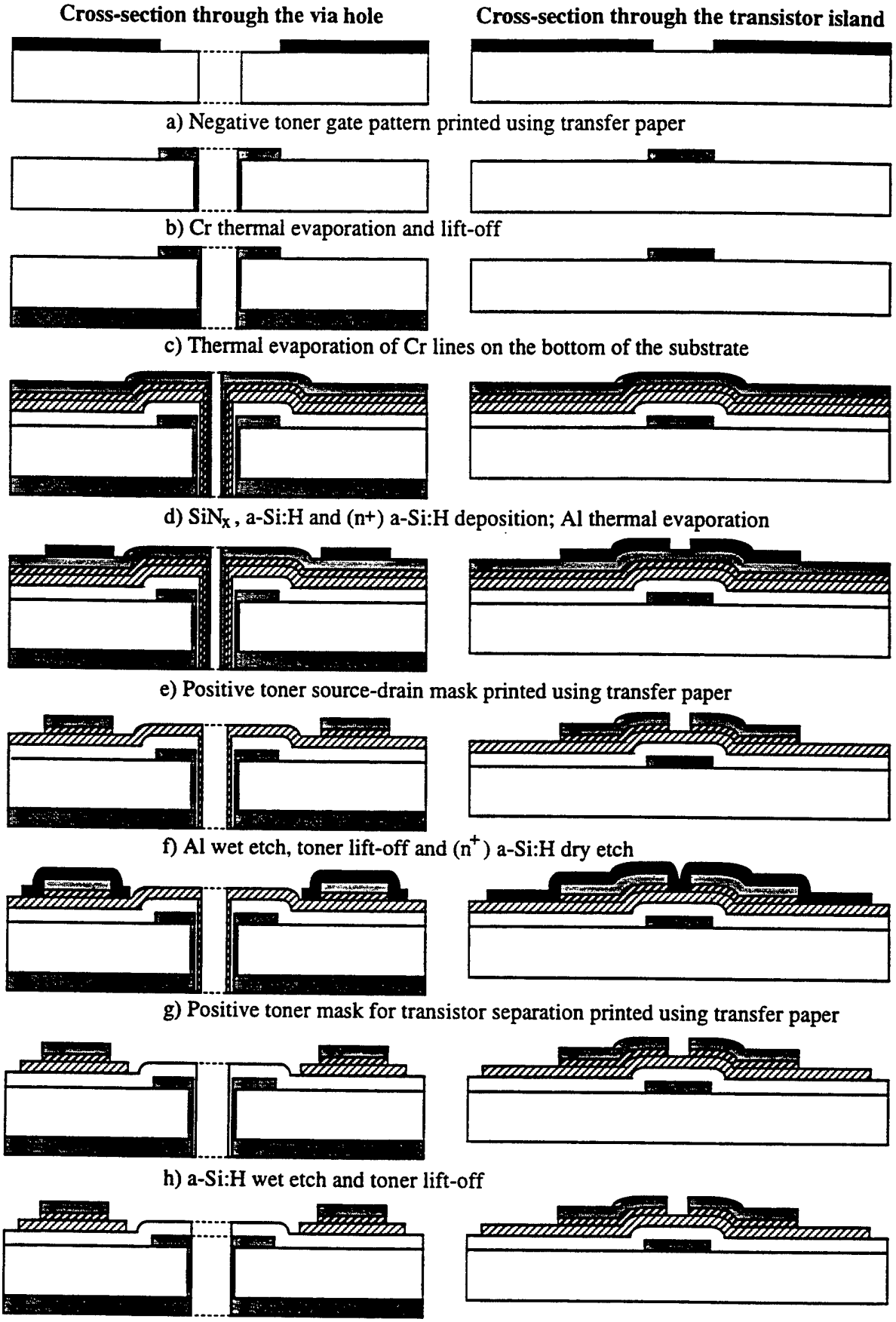


Figure 4. Process sequence

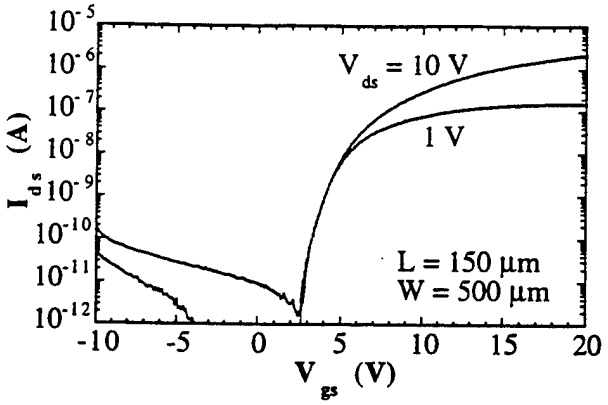


Figure 5. Source-drain current as a function of gate voltage for V_{ds} = 1 V and 10 V. The source electrode is grounded.

Results and discussion

The dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for V_{ds} = 1 V or 10 V is shown in Fig. 5. During the measurement the gate voltage was applied from the bottom through the via hole. The off-current is ~ 1 x 10^{-11} A and the ratio of the on-off current is $\geq 10^5$. These values reflect an immature process technology but demonstrate the feasibility of the via hole concept. In the linear approximation the source-drain current is given by:

$$I_{ds} = \frac{W}{L} C_{SiN} \mu_n \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

where L is the channel length, W the channel width, C_{SiN} the capacitance of the gate insulator, μ_n the electron mobility, and V_T the threshold voltage. At V_{ds} = 1 V we obtain V_T ~ 4.5 V and a value 1.53 x 10^{-8} A V^{-1} for the (C_{SiN} μ_n V_{ds} W / L) product. Using C_{SiN} = 1.38 x 10^{-8} F cm^{-2} we calculate a linear mobility of ~ 0.33 cm^2 V^{-1} s^{-1}.

We compared the TFT characteristics measured with the gate voltage applied to the bottom with the characteristics measured with the gate voltage applied to the top. No change was observed. The resistance through the via hole was ~ 1 kΩ due to thin sidewall coverage by the evaporated Cr. We reduced the resistance through the hole by ~ 2 orders of magnitude by soldering In into the via hole.

Summary

We demonstrated a technique that allows a large increase of the size of active matrix backplanes by reducing the gate line RC. This technique consists of introducing via holes. We fabricated via holes of 30 to 40 µm diameter in a 50 µm glass foil. An array of amorphous silicon thin-film transistors was made on a thin glass substrate with via holes, using a process where all pattern definition steps use electrophotographic toner masks. All the gates are connected through via holes to a metal line that is run on the bottom of the substrate. The transistor gates were addressed with contacts made to the bottom metal. Thus we have demonstrated a new technology for RC gate delay reduction in large-area displays.

This work is supported by DARPA through WPAFB under Contract F33615-94-1-4448, and by EPRI.

References

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2. H. Gleskova, R. Könenkamp, S. Wagner and D.S. Shen, IEEE Electron Device Lett. 17 (1996) 264.

VIA-HOLE ADDRESSED TFT AND PROCESS FOR LARGE-AREA a-Si:H ELECTRONICS

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ABSTRACT

We demonstrate a new technology for RC gate delay reduction, by fabricating an array of amorphous silicon thin-film transistors (a-Si:H TFTs) on a thin glass substrate provided with via holes. All gates are connected through via holes to a metal line that is run on the back side of the substrate. We opened via holes with a diameter of 35 to 50 μm in 50 μm glass foil. For the first time, *all* TFT pattern definition steps used a process which employs electrophotographic toner masks.

INTRODUCTION

Active matrix liquid crystal displays (AMLCDs) are a key application of large-area circuits based on thin film transistors (TFTs). With standard inverted-staggered amorphous silicon based TFTs, the size of the AMLCD's TFT backplane is restricted by the RC time constant of the bottom gate conductor [1]. To ensure good step coverage by the overlying TFT layers, the thickness of this gate conductor is limited to ~ 300 nm, and it must be kept narrow to provide a large pixel aperture. As a consequence, the projected limit for AMLCD diagonal size is ~ 40 inches [1]. Yet, very large AMLCDs are desirable products because of their excellent image quality. Therefore, we have been developing printing techniques to reduce the manufacturing cost of backplanes for such large AMLCDs [2,3].

Here we show how the size restriction on a display that results from the RC time constant for the bottom metal line can be relaxed. In a-Si:H TFTs the bottom metal usually is the gate. We open via holes through the substrate, and connect the TFT gates on the front side with a gate line that is run on the back side of the substrate. Because this line is not part of the semiconductor structure, it can be made much thicker than on the front. As a result, the gate RC delay can be reduced greatly.

Fig. 1 shows a simple model of display line resistance. In figure 1a a line with resistance R is driven from a source on the left side. Figure 1b shows that if a perfect conductor is added in parallel on the back side of the glass and linked to the front metal at the edges of the plate, the highest resistance R_{max}, to the center of the line, becomes R/4. In fact, this is equivalent to driving the line from both the left and the right ends. In the following discussion we will concentrate on driving from only one end. For a non-ideal back line of total resistance of R/n (Figure 1c), it can be shown that R_{max} and its position x_{max} are as follows:

$$R_{max} = \frac{R}{4}\left(1 + \frac{1}{n}\right), \quad x_{max} = \frac{1}{2}\left(1 + \frac{1}{n}\right)$$

It is clear that when n becomes large (perfect conductor or line driven from both ends), R_{max} approaches R/4, and the point of highest resistance is shifted to the center.

If via holes are added along the line and contacts are made through the holes to the back side conductor, the highest resistance R_{max} is located in the section farthest from the source, and is given by:

$$R_{max} = \frac{R\,(m-1)}{m\,(1+n)} + \frac{R}{4m}\left(1 + \frac{1}{n}\right)$$

Here m is the number of line segments, and (m+1) is the number of front-to-back connections.

Fig. 2 shows R_{max}/R as a function of n, using m as parameter. Two points are clear from the figure. First, when the resistance of the back line is reduced, the resistance drops rapidly first, and then saturates near n=10: when the back resistance becomes one order of magnitude lower than the resistance of the front line, reducing it further has no perceptible effect. Second, not many via holes are needed to reduce the resistance. Five via holes (m=4) with a thick back line (e.g. n=5) bring the maximum resistance down to ~ 20% of the front-line-only value. Conversely, this particular configuration would allow increasing the panel size by a factor of 5, as shown by the scale on the right ordinate of Fig. 2.

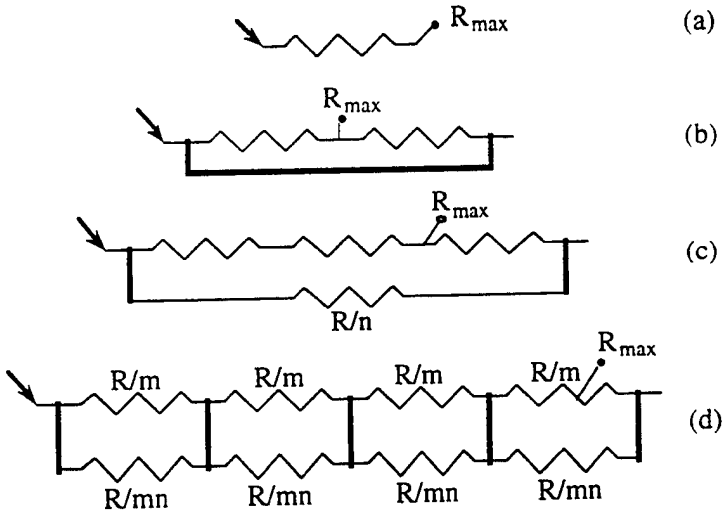


Figure 1. Equivalent circuit of front and back gate conductors with via hole connections (vertical bars), (a) line driven from one side, (b) connection at both plate edges to a perfect conductor on the back, (c) same as (b) but non-perfect back conductor, (d) general case.

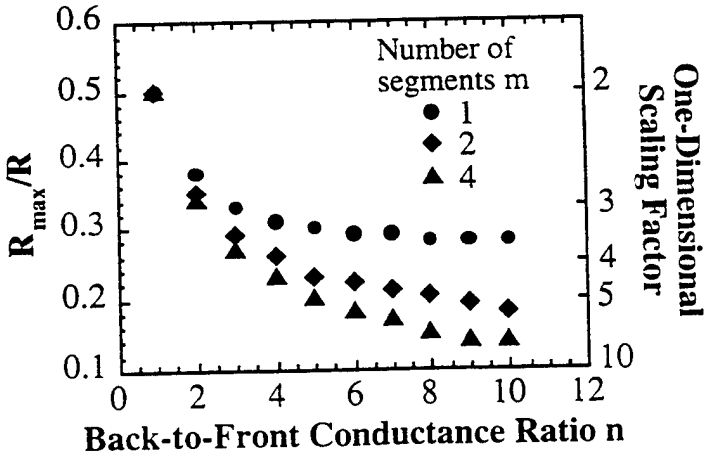


Figure 2. Effect of the back wire resistance R/n and of the number m of via holes on the normalized maximum resistance (left scale) and on the scaling factor for display size (right scale).

EXPERIMENTAL PROCEDURES

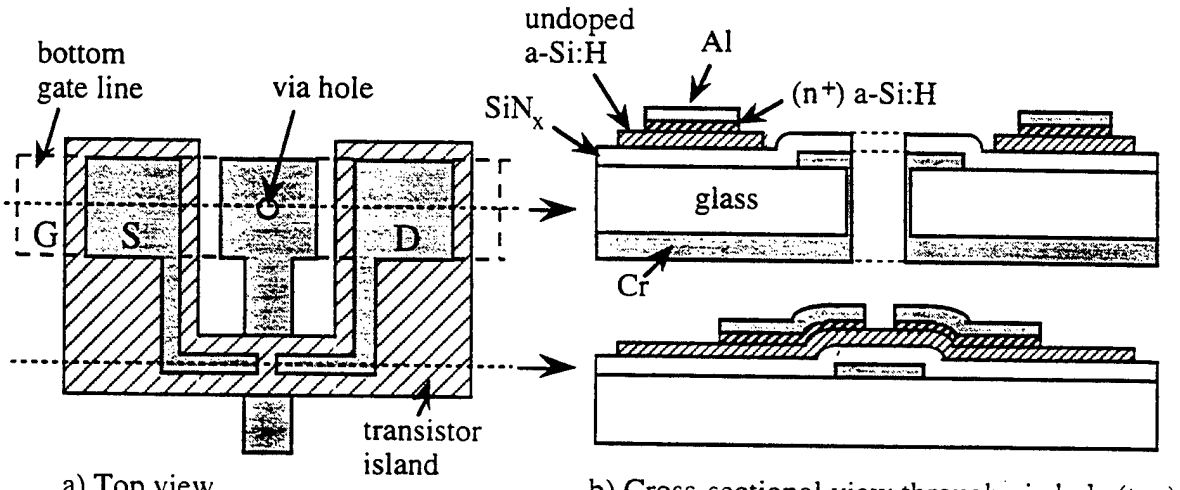
The via holes were fabricated in a 50 μm glass foil (Schott # AF 45) by drilling [4] with an ArF excimer laser (λ = 193 nm). The holes were drilled from either one or two sides. Laser drilling from one side provided funnel-shaped holes with entrance and the exit hole diameters of ~ 70 μm and ~ 35 μm, respectively.

The TFTs have a bottom gate, back-channel etch structure. Our simple process requires only three different patterning steps. Each patterning step uses a mask of laser printed toner [2,3]. The gate conductor pad of each TFT is collocated with a via hole, through which each gate is connected to the Cr line run on the back side of the substrate. A 3 x 1.5 $in.^2$ glass substrate with 32 two-side drilled via holes was used. A top and two cross-sectional views of the TFT structure are shown in Fig. 3.

The schematic all-toner mask process sequence is shown in Fig. 4. First, we printed a negative toner gate mask on the glass substrate using transfer paper [3]. The transfer paper procedure is very similar to the one published before [3] except now we do not use photoresist as adhesion layer. Then a ~ 100 nm thick Cr layer was thermally evaporated and the toner was lifted-off in PRX 100 stripper. The back side ~ 200 nm thick Cr gate lines were thermally evaporated through a metal mask.

After the front-to-back Cr connections were fabricated, we deposited a sequence of the following layers in a multi-chamber deposition system: ~ 450 nm of SiN_x, ~ 250 nm of undoped a-Si:H, and ~ 50 nm of (n^+) a-Si:H. An ~ 100 nm thick Al layer was thermally evaporated. We printed a positive source-drain toner pattern using transfer paper [3]. Then the Al layer was wet etched, the toner was stripped-off, and the (n^+) a-Si:H layer was dry etched in CF_4 gas. Next, we printed a positive toner mask for transistor separation, again using transfer paper. The undoped a-Si:H layer was etched in KOH solution, and the toner was stripped off. Finally, we dry-etched the substrate from the back side to remove any SiN_x from the holes.

After the fabrication, the TFTs were annealed at 200°C for 30 min. in forming gas.



a) Top view

b) Cross-sectional view through via hole (top) and through TFT (bottom).

Figure 3. Top and cross-sectional views of one TFT.

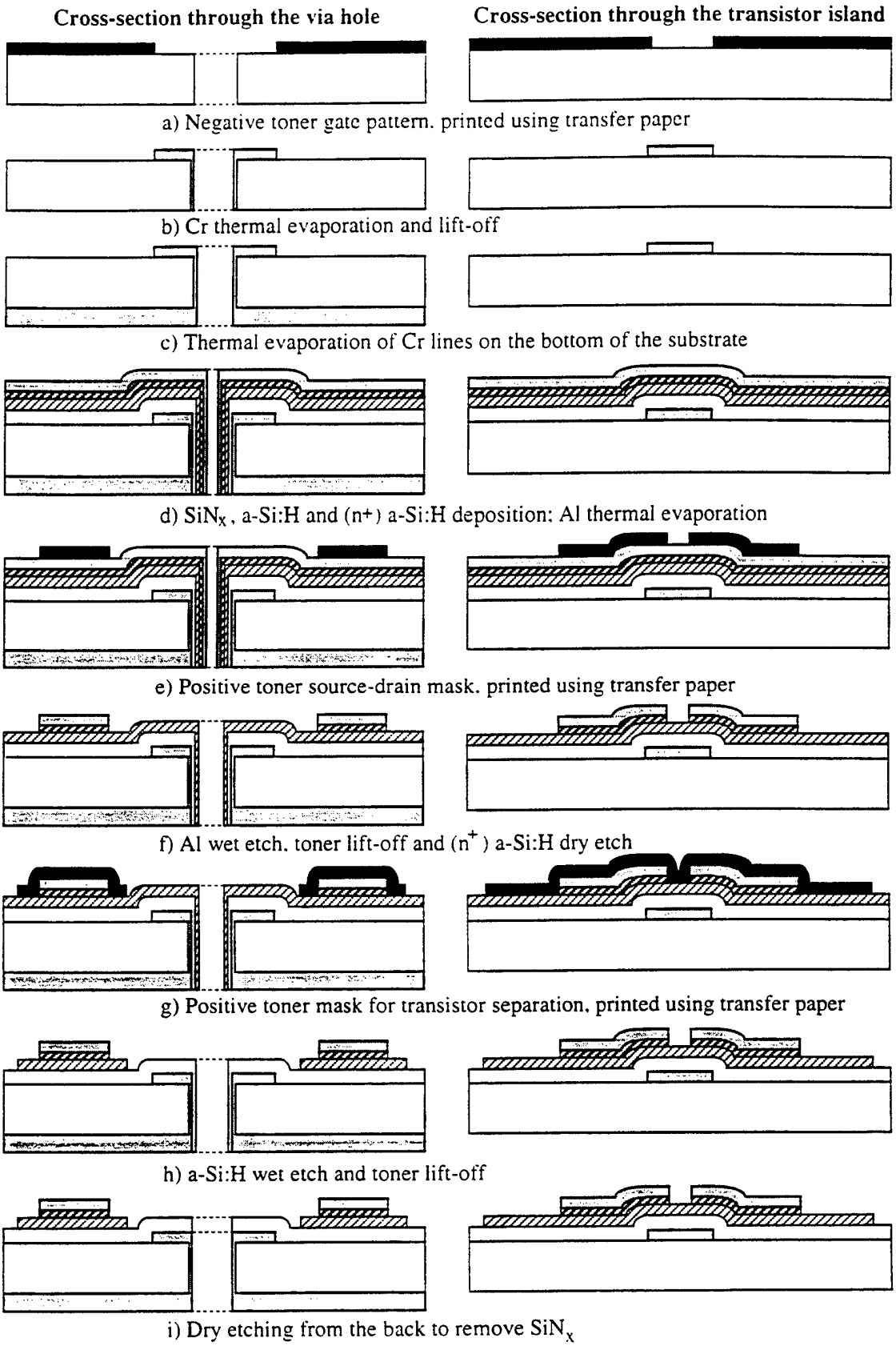


Figure 4. Process sequence

RESULTS AND DISCUSSION

The dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for V_{ds} = 1 V or 10 V is shown in Fig. 5. The gate voltage was applied from the bottom through the via hole. The off-current is ~ 3 x 10^{-12} A and the on-off current ratio is ~ 10^6. These values are comparable with those of a-Si:H TFTs fabricated using conventional photolithography and demonstrate the feasibility of the via hole concept.

In the linear approximation the source-drain current is given by:

$$I_{ds} = \frac{W}{L} C_{SiN} \mu_n \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

where W is the channel width, L the channel length, C_{SiN} the capacitance of the gate insulator, μ_n the electron mobility, and V_T the threshold voltage. At V_{ds} = 1 V we obtain V_T ~ 2.8 V and a value 1.89 x 10^{-8} A V^{-1} for the (C_{SiN} μ_n V_{ds} W / L) product. Using C_{SiN} = 1.38 x 10^{-8} F cm^{-2} we calculate a linear mobility of ~ 0.41 cm^2 V^{-1} s^{-1}.

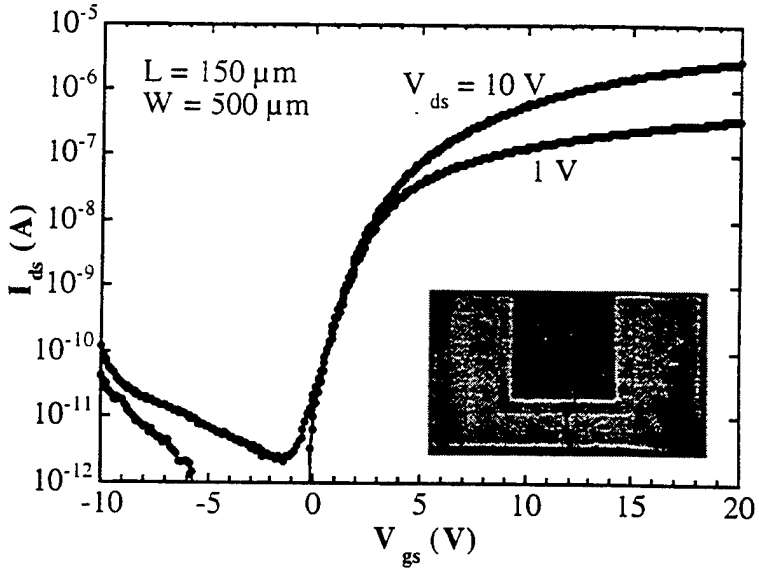


Figure 5. Source-drain current as a function of gate voltage for V_{ds} = 1 V and 10 V. The source electrode is grounded. The insert is photograph of a TFT with a via hole (black dot in gate contact pad). The Cr line on the back side is the wide horizontal conductor underneath the gate contact pad.

We compared the TFT characteristics measured with the gate voltage applied to the bottom with the characteristics measured with the gate voltage applied to the top. No difference was observed. The resistance through the via hole was ~ 1 kΩ due to thin sidewall coverage by the evaporated Cr. We reduced the resistance through the hole by ~ 2 orders of magnitude by soldering In into the via hole.

SUMMARY

We demonstrated a technique that allows a large increase of the size of active matrix backplanes by reducing the gate line RC. This technique consists of introducing via holes. We

fabricated via holes of 35 to 50 μm diameter in a 50 μm glass foil. An array of amorphous silicon thin-film transistors was made on this thin glass substrate. We made the TFTs with a process where all pattern definition steps use electrophotographic toner masks. All the gates are connected through via holes to a metal line that is run on the back side of the substrate. The transistor gates were addressed with contacts made to the back side metal. Thus we have demonstrated a new technology for RC gate delay reduction in large-area displays.

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4. Resonetics, Inc., 4 Bud Way, Suite 21, Nashua, NH 03063.

Via Hole Technology for Thin-Film Transistor Circuits

H. Gleskova, S. Wagner, Q. Zhang, and D. S. Shen

Abstract—We analyze and demonstrate a new technique for reducing the gate RC delay of the amorphous silicon thin-film transistor (TFT) backplane of active matrix liquid crystal displays. The TFT gate line is driven from a bus on the back side of the glass substrate, through a laser-drilled via hole. Analysis shows that a few via holes suffice to considerably reduce the gate RC delay, or enable an equivalent increase in display size.

THE SIZE of the TFT backplane for active matrix liquid crystal displays (AMLCD's) is restricted by the RC delay of the bottom conductor [1], which in the standard inverted-staggered amorphous silicon TFT structure is the gate metal. To ensure good step coverage by the overlying insulator and semiconductor layers, the thickness of this gate conductor is limited to ~300 nm, and it must be kept narrow to provide a large pixel aperture. The maximum diagonal using low-conductivity metals [2], [3] is projected at ~40 in [1].

Here we show that the gate RC delay can be reduced considerably, and the AMLCD's be made correspondingly larger, by connecting the gate line through a few via holes to a bus run on the back side of the substrate. This bus can be much thicker than the gate line on the front side, because it is not part of the semiconductor structure.

First we analyze driving the gate line from a source at one edge of the display, with the bus at the back side connected only at the two edges. When the resistance of the back side bus is R/n of the front side conductor resistance R, the maximum resistance R_{max} of the gate line, and its position as a fraction of gate line length x_{max}, are given by

$$R_{max} = \frac{R}{4}\left(1+\frac{1}{n}\right), \quad x_{max} = \frac{1}{2}\left(1+\frac{1}{n}\right). \qquad (1)$$

When n becomes large (perfect backside conductor) R_{max} approaches $R/4$, and the point of highest resistance is brought to the center of the gate line. When additional connections between the gate line and the back side bus are made through via holes, R_{max} becomes located in the section farthest from the source, and is given by

$$R_{max} = \frac{Rm}{(m+1)(n+1)} + \frac{R}{4(m+1)}\left(1+\frac{1}{n}\right). \qquad (2)$$

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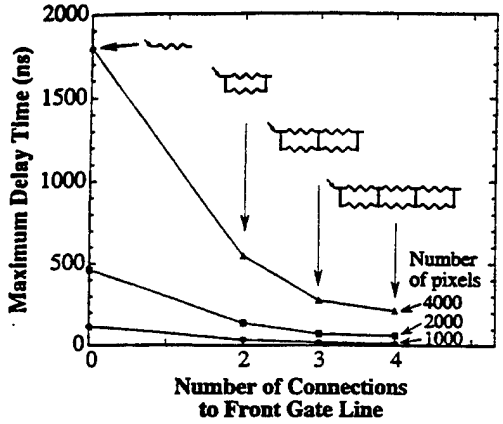

Fig. 1. Maximum gate delay calculated for conventional addressing from one edge, and as a function of the number of back-to-front connections, for three different pixel numbers. See text for circuit specifications.

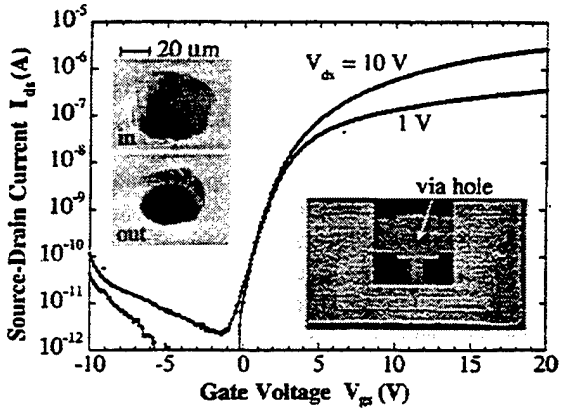

Fig. 2. ON/OFF characteristics of the TFT ($L = 150$ μm, $W = 500$ μm) shown in the right inset. Note via hole (black dot) in gate pad (center), connecting to the horizontal back side bus visible through the glass. Rough edges result from ~10 μm size toner particles. Left inset: SEM photographs of laser drilled via hole in the 50-μm glass.

Here m is the number of via holes, and the total number of front-to-back connections is $m+2$. Thus, when the resistance of the back conductor is reduced (n is raised), R_{max} drops quickly first, and saturates when the back resistance becomes one order of magnitude lower than the front resistance. Note that not many via holes are needed to reduce R_{max}.

We also simulated the effect of inserting via holes on dynamic performance. Earlier simulations have shown that a-Si:H TFT's are suitable for large-area high-resolution AMLCD's [1], [4] and that the TFT performance does not

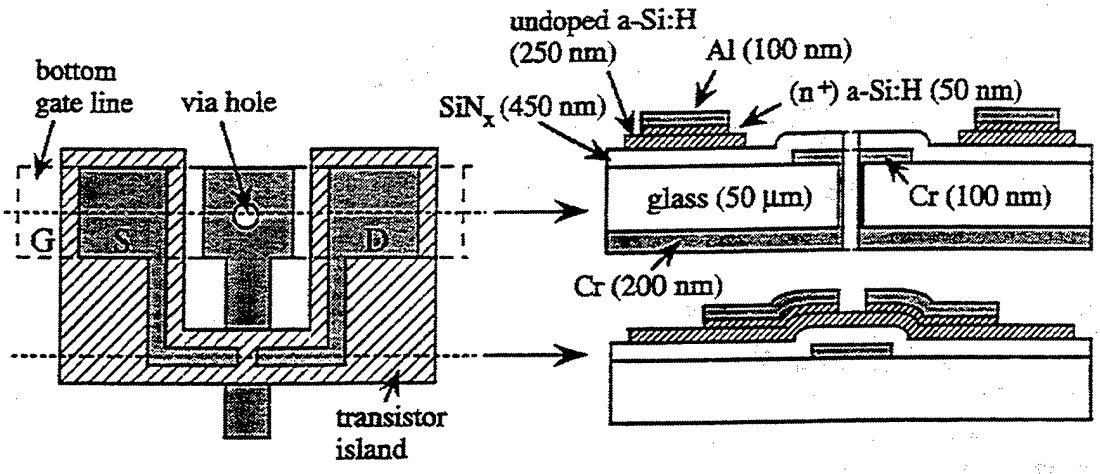

Fig. 3. Schematic top and cross-sectional views of the TFT with a via hole in the gate pad.

control delay [1]. We used SPICE to model the maximum gate line delay time of our new via hole structure in large displays, with up to 4000 pixels per line [5]. We modeled the gate line as lumped sections of resistor and capacitor chains, bounded by via hole connections. For the section where the maximum delay appears we used a distributed model with pixel resistance and pixel capacitance. Depending on substrate thickness, the front-to-back capacitance is 0.2–2 fF/pixel, and the back side interline capacitance is <1 fF/pixel. Both are negligible in comparison to the pixel capacitance of typically 300 fF. We examined the relationship between delay and all important circuit parameters, including the unit pixel resistance, the pixel capacitance, the front-to-back resistance ratio, and the number of via holes. Fig. 1 shows the maximum gate delay time versus the number of front-to-back connections for three different pixel numbers per line, using 1 Ω pixel resistance, 300 fF pixel capacitance, and a front-to-back conductor resistance ratio of 10. This figure demonstrates the reduction in delay when raising the number of connections from (0)—drive from one edge, over (2)—back conductor and drive from both edges, to (3) and (4)—one and two via holes. For a large display, a front-to-back resistance ratio of 10 and two via holes in each line reduce the delay time to 1/7–1/8. Correspondingly, the panel size can be increased by a factor of 7–8.

We used 3×1.5 in^2 50-μm thick glass foil (Schott #AF 45) as the substrate for a-Si:H TFT fabrication. An 8×4 matrix of via holes was drilled [6] from either one or both sides using an ArF excimer laser ($\lambda = 193$ nm). The laser pulse energy was 70 mJ, fluence 11 J/cm^2, repetition rate 100 Hz, and ~1100 laser pulses were needed for drilling one hole. Drilling from one side produced funnel-shaped holes with entrance and exit hole diameters of ~70 μm and ~35 μm, respectively (Fig. 2).

To demonstrate the feasibility of laser drilling for third-generation AMLCD glass substrates, we also drilled holes into 0.5 mm thick Corning 7059 glass, again from either one or both sides. The pulse energy was 140 mJ, fluence 30 J/cm^2, repetition rate 50 Hz, and ~4300 pulses were required for one hole. Drilling from one side made funnel-shaped holes with entrance and exit diameters of ~40 μm and ~10 μm, respectively.

The bottom gate, back channel etched TFT's were fabricated using an all printed-toner patterning process [7], which is the first time that TFT's have been made with all-printed masks. Because our present mask printing process requires a flexible substrate, we employed the 50-μm glass foil to demonstrate the via hole geometry. Each chromium gate pad on the front side of the substrate is collocated with a via hole for connection to a Cr bus run on the back side. The front-to-back connections through the via holes were made by two Cr evaporations, front and back, producing an ~1 kΩ through-resistance. In recent experiments we have reduced the through-hole resistance by 2–3 orders of magnitude with In filling or electroless-plated Cu. A top and two cross-sectional views of the TFT structure are shown in Fig. 3. The complete fabrication sequence is described elsewhere [8].

The ON/OFF characteristics of a TFT addressed from the back side through a via connection are shown in Fig. 2. The off-current is $\sim 1 \times 10^{-14}$ A/μm, and the ON/OFF ratio is $\sim 10^6$. In the linear approximation at $V_{ds} = 1$ V we obtain $V_{\text{Threshold}} \sim 2.8$ V and an electron mobility of ~0.41 cm^2 V^{-1} s^{-1}. These values are comparable to those of a-Si:H TFT's fabricated using conventional photolithography, and demonstrate the feasibility of the via hole concept (and of printed-toner masks).

The via hole concept can be applied to other types of substrates considered for macroelectronics. Front-to-back connections can be made through mechanically punched holes in polyimide foil substrates as for a-Si:H based flexible solar modules [9], and the etching of holes is well established for steel foils [10], which have been demonstrated as substrates for TFT-driven organic light-emitting diodes [11].

In summary, we demonstrated a technique for increasing the size of AMLCD backplanes by reducing the gate RC delay. This technique consists of addressing the gates through via hole connections. Analysis shows that even a small number of via holes can have a large effect. We laser drilled via holes in 50-μm and 0.5-mm thick glass. An array of a-Si:H transistors was made on the 50-μm glass foils, using a new process where all pattern definition steps rely on electrophotographically printed toner masks. The transistor gates were addressed from the back side of the substrate through the via holes. Thus

we have demonstrated a new technology for RC gate delay reduction of particular benefit to large-area displays.

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Modeling of Gate Line Delay in Very Large Active Matrix Liquid Crystal Displays

Qing Zhang, D. S. Shen, H. Gleskova, and S. Wagner

Abstract—**With standard inverted-staggered amorphous silicon based TFT's, the size of active matrix liquid crystal displays is restricted by the RC time constant of the gate conductor. This RC delay can be reduced considerably by connecting the gate line through via holes to a bus run on the back side of the substrate. We use the SPICE model to examine the relationship between the RC delay and all important circuit parameters. The results show that with a low-resistance back line and only a few via holes per line, the delay can be reduced by nearly a factor of ten.**

I. Introduction

With standard inverted-staggered amorphous silicon based TFT's, the diagonal of the AMLCD's TFT backplane is restricted by the RC time constant of the gate conductor [1]. Recently, we proposed that the gate line RC delay can be reduced considerably, and the AMLCD's be made correspondingly larger, by connecting the gate line through a few via holes to a bus run on the back side of the substrate [2]. This bus can be made much thicker than the gate line on the front side, because it is not part of the semiconductor structure (Fig. 1).

The new gate line powered through via holes can be modeled as a modified RC delay line consisting of a cascade of two-port networks of finite pixels, as shown in Fig. 2. Each two-port network represents one section of the line, which has via holes at both ends. It is obvious that the gate line pulse suffers distortion as it moves through the line. The distortion increases the rise time and delays the arrival of the gate pulse. The delay can cause the gate and data pulses to arrive at a pixel out of synchronization. In this paper, the longest time interval during which the pixel voltage takes to rise from 0 to 50% of its final voltage is defined as the maximum delay time T_m when the input is an ideal step signal. In a classical RC line model the maximum delay time appears in the last pixel. A well-known equation is generally used to describe the behavior of an RC transmission line [3].

However, our new structure has a back conductor. Because the low-resistance back line is connected in parallel with the RC net, the delay time does not appear in the last pixel of the gate line. Actually, the maximum delay is experienced by a certain pixel in the last section.

II. Results of Spice Simulation

We use numerical results based on SPICE simulation to expose the relationship between the maximum delay time and the physical parameters of the new structure.

A. Maximum Delay Time versus Pixel Resistance R and Capacitance C

In Fig. 3, the maximum delay time is plotted for pixel resistance R ranging from 0.5 to 10 Ω. The case labeled "no cross-res" is a classical single-sided RC transmission line. The other cases are the new structure with back line and via holes. The top and back lines are connected at the edge. It is clear that the delay time depends linearly on the resistance in all cases. Comparing the case of no back line with the via hole structure makes clear that the dependence on pixel resistance has been drastically reduced. Similarly, the relationship between the delay time and pixel capacitance also is a linear function. Again we note that a small number of via holes can drastically suppress the effect of a larger RC.

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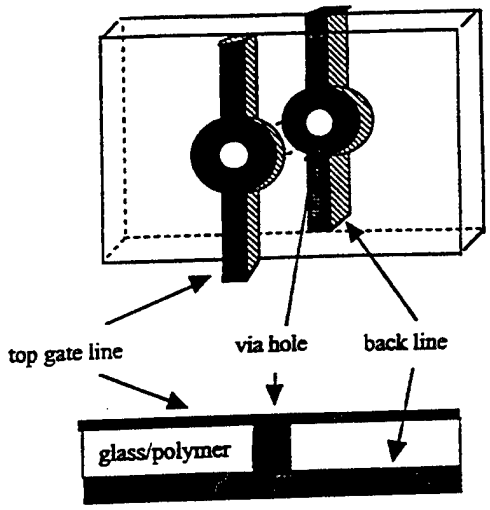

Fig. 1. Scheme of via holes, top gate line, and back line.

B. Maximum Delay Time versus Resistance r of Back Line

Here, the discussion is based on the ratio K of the section resistance R' (top line) to r (back line). It is clear that a larger K will greatly reduce the delay time (Fig. 4). For example, if $R = 1\ \Omega, C = 300$ fF, $N = 1000$, the delay time will drop from 61 to 16.6 ns when K is increased from 1 to 10, for two via holes in the line. In fact, it is preferred to keep K small so that we can deposit back lines with practical thickness. Here, we show that it is not necessary to make K very large, because of the diminishing return of raising K above 10.

C. Maximum Delay Time versus the Number of via Holes L

Fig. 5 shows the simulation result. It demonstrates that a small number of via holes, or even a back line connected at both ends to the top line ("0 hole"), can drastically reduce the delay. Increasing the number of holes beyond one provides additional reduction, but not many holes are required.

D. Maximum Delay Time versus the Number of Pixels N

It is clear that the larger the number of pixels N, the longer the delay time. This is evident from Fig. 5. As the liquid crystal display area becomes large and resolution becomes high, the number of pixel becomes correspondingly larger. Using the via hole technology, it is possible to reduce the delay time substantially. For example, if we take $L = 2, K = 10, R = 1\ \Omega, C = 300$ fF, then the delay time is 0.21 μs for $N = 4000$. For a classical RC line with the same R, C, and N, it would be 1.8 μs.

III. Analysis and Discussion

Here, we will derive a semi-experimental expression for T_m and discuss it further. Assuming that the output resistance R_0 of driving

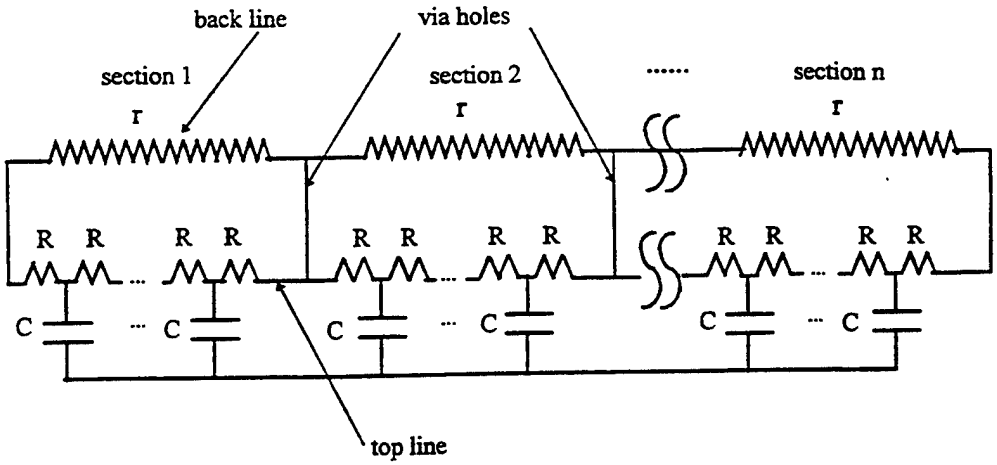

Fig. 2. The circuit model. Here R and C are the pixel resistance and capacitance, respectively. r is the resistance per section of back line.

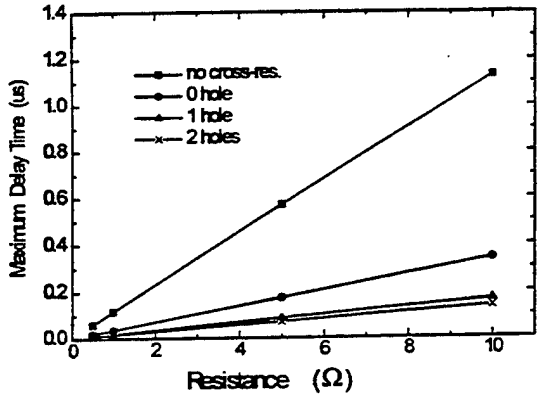

Fig. 3. Maximum delay time versus unit pixel resistance R. Here, $C = 300$ fF, $N = 1000$, and $K = 10$.

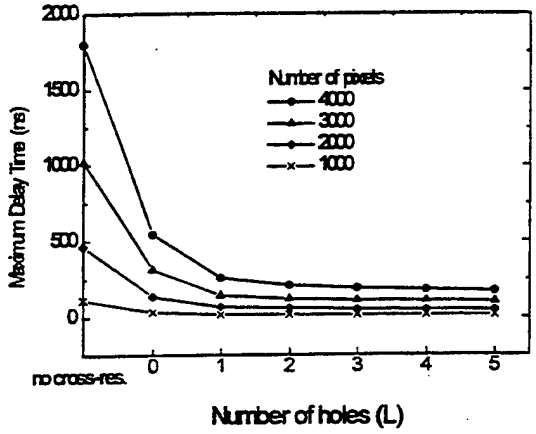

Fig. 5. Maximum delay time versus the number of holes L. Here, $R = 1\ \Omega, C = 300$ fF, and $K = 10$.

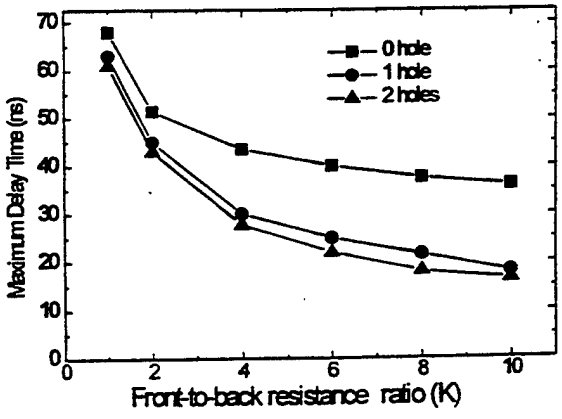

Fig. 4. Maximum delay time versus resistance ratio K, which is the total section resistance R' of top line versus back line resistance r. Here, $R = 1\ \Omega, C = 300$ fF, and $N = 1000$.

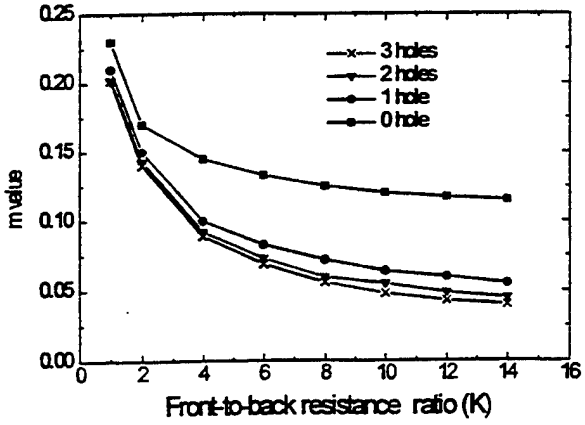

Fig. 6. The m value versus resistance ratio K and the number of holes L.

source is zero, the delay time T_m can be expressed approximately as

$$T_m \approx mRCN^2 \tag{1}$$

where R, C, and N are the same as that in Section II. Here m is a coefficient, determined by both the resistance ratio K and the number of via holes L. The value of m is plotted in Fig. 6. Note that the m value here is derived from SPICE simulation without an explicit expression. However, it is possible to derive an explicit equation for m from circuit theory, the details will be reported later.

For a constant number of via holes, the delay time is determined by the resistance ratio K. The curves levels off for $K > 10$. Similarly, if we keep K constant, the delay time is decided by the number of via holes L. Since the curve for $L = 3$ is very close to that of $L = 2$, two via holes appears to be an acceptable choice.

Therefore, for $L = 2, K = 10$, (1) can be simplified to

$$T_m \approx (0.045 \sim 0.055)RCN^2. \quad (2)$$

For comparison, the delay time of a classical RC transmission line is [4]

$$T_m \approx 0.38RCN^2. \quad (3)$$

Comparing (2) with (3), we see that via hole technology will reduce the response time of the gate line by about one order of magnitude.

IV. Conclusions

1) The gate line connected through via holes can be modeled as a modified RC transmission line, which consists of a cascade of several sections of two-port networks.
2) Numerical results based on simulation provide approximate relationships between the delay time and electrical and geometrical parameters. RC constant, number of via holes L, front-to-back resistance ratio K, and total number of pixel N are important factors for the determination of the delay time. A front-to-back resistance ratio K of 10 and 2 via holes in each line reduce the delay time to one-seventh to one-eighth.

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Numerical modeling of the dependence of the steady-state photoconductivity in hydrogenated amorphous silicon on the rate of carrier generation

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The photoconductivity σ_{ph} of hydrogenated amorphous silicon measured in experiments has a power law dependence on the carrier generation rate G: $\sigma_{ph} \propto G^{\gamma}$. The exponent γ is often interpreted as a measurement of the density of states distribution in the upper half of the band gap. This paper reports the numerical modeling of the dependence of the photoconductivity on the carrier generation rate. Examination of the traditional closed form solution shows that for the important case of γ close to unity, numerical modeling is required. The results of such numerical modeling show that γ is more sensitive to the *total number* of gap states rather than the *distribution* of states. A γ close to unity is better interpreted as a supplementary indication of low total defect density in the upper half of the band gap, instead of a certain distribution of these states. © *1995 American Institute of Physics.*

I. INTRODUCTION

Photoconductivity is an important material parameter of hydrogenated amorphous silicon (a-Si:H). Because the recombination centers are distributed in the band gap, the photoconductivity increases sublinearly with the carrier generation rate G. The measured photoconductivity σ_{ph} is found to depend on G:

$$\sigma_{ph} \propto G^{\gamma}. \tag{1}$$

The exponent γ usually lies between 0.7 and 1.0. Figure 1 shows the value of this photoconductivity exponent γ, measured on a large sample pool of hydrogenated amorphous silicon. The i layers employed in high-efficiency amorphous silicon solar cells usually have value of γ close to unity, typically above 0.95. (The situation in alloys of a-Si:H is more complicated and will not be discussed in this paper). A low γ of the i-layer material leads to a low cell efficiency via a low fill factor, and often can be traced back to certain unoptimized deposition conditions or to small leaks in the deposition system. Thus it appears that the value of γ is related to the density of defect states in the material.

Models have been developed to describe the photoconductivity in semiconductor materials including hydrogenated amorphous silicon.[1-6] Closed-form solutions were derived for some cases.[1,6] However, because of the complexity of the distribution of the band-gap states, a closed-form solution cannot be always derived, so that a numerical model is needed. This paper reports our results of numerically modeling the carrier generation rate dependence of the photoconductivity. The applicability and limits of the traditional closed-form solution are discussed first. Then we introduce the numerical model, and present and discuss the results of the modeling.

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II. ANALYTICAL MODEL AND LIMITATION OF ITS CLOSED-FORM SOLUTION

A complete steady-state photoconductivity model for semiconductor materials including hydrogenated amorphous silicon was developed by Rose.[1] In this model, the steady-state photoconductivity is determined by the free electron density n and their band mobility μ_0:

$$\sigma_{ph} = nq\mu_0. \tag{2}$$

Here q is the electron charge. We did not include the hole contribution because the hole mobility is low, so that their contribution to the photocurrent is small.

In steady state, the carrier generation rate G equals the recombination rate. This condition determines the free electron density:

$$n = G\tau. \tag{3}$$

Here τ is the lifetime of free electrons.

The free electron lifetime depends on the recombination centers in the band gap. Under illumination, the quasi-Fermi levels split. The states between the dark Fermi level E_{fo} and the electron quasi-Fermi level E_{fn} become occupied and become recombination centers.[1] Thus,

$$\tau = \frac{1}{v_{th}\int_{E_{f0}}^{E_{fn}} \sigma N(E)dE}. \tag{4}$$

Here v_{th} is the electron thermal velocity, σ the capture cross section, and $N(E)$ is the density of states in the band gap.

On the other hand, the quasi-Fermi level E_{fn} is a quantity that describes the free electron density:

$$n = N_c \exp\left(-\frac{E_c - E_{fn}}{kT}\right). \tag{5}$$

Here N_c is the effective density of states in the conduction band, kT is the thermal energy, and E_c is the energy of the conduction-band edge.

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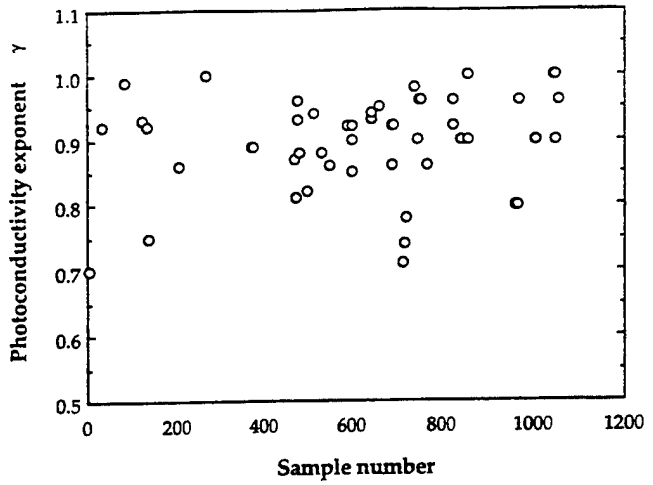

FIG. 1. The photoconductivity exponent γ of a large pool of a-Si:H samples demonstrate that γ typically lies between 0.7 and 1.0.

From Eqs. (3)–(5) we obtain

$$N_c \exp\left(-\frac{E_c-E_{fn}}{kT}\right)=\frac{G}{v_{th}\int_{E_{f0}}^{E_{fn}}\sigma N(E)dE}. \tag{6}$$

A closed-form solution can be derived for certain distributions of the density of states $N(E)$, including exponential distribution:

$$N(E)=N_0 \exp\left(-\frac{E_c-E}{kT_c}\right). \tag{7}$$

Here N_0 and kT_c are parameters that describe the density of states and its distribution. Since the derivation of the closed-form solution is important for the following discussions, we will carry it out here.

After substitute $N(E)$ with Eq. (7), assuming that σ is a constant, we carry out the integral in Eq. (6) to obtain

$$N_r=kT_cN_0\left[\exp\left(-\frac{E_c-E_{fn}}{kT_c}\right)-\exp\left(-\frac{E_c-E_{f0}}{kT_c}\right)\right]. \tag{8}$$

Here N_r is the total number of states under the integral. Assuming that the second term is negligible compared to the first term, we have

$$N_r\approx kT_cN_0 \exp\left(-\frac{E_c-E_{fn}}{kT_c}\right). \tag{9}$$

From Eqs. (2), (5), (6), and (9), we have the carrier generation rate dependence of the density of free electron n, and of the photoconductivity σ_{ph}:

$$\sigma_{ph}\propto n\propto G^{T_c/(T+T_c)}. \tag{10}$$

Thus γ traditionally has been interpreted as the ratio of T_c to $(T+T_c)$:

$$\gamma=\frac{T_c}{T+T_c}. \tag{11}$$

Since T_c is a parameter that describes the exponential distribution of the density of states, often information about the distribution of the density of states is extracted from γ.

The midgap states in amorphous silicon are better described by a Gaussian[7] than an exponential distribution, but usually the exact form of the distribution is not important as long as one can assume that at least over a limited range the density of states is exponential. However, in some cases, especially for materials with a γ close to unity, we need to have a closer look at the consequences of Eq. (8).

According to Eq. (11), $\gamma\approx 1$ suggests a flat distribution of density of states ($kT_c\rightarrow\infty$). However, inspection of Eq. (8) suggests that in this case we cannot omit the second term. Comparison of the two terms in Eq. (8) makes clear that the condition for omitting the second term is

$$\exp\left(\frac{E_{fn}-E_{f0}}{kT_c}\right)\gg 1 \tag{12}$$

or

$$E_{fn}-E_{f0}\gg kT_c. \tag{13}$$

This condition can be satisfied easily when kT_c is small. However, if kT_c is large (e.g., in the case of $\gamma\approx 1$), error is introduced. For example, if γ is 0.97, at room temperature, kT_c must be 0.87 eV. Now, to satisfy condition (13) we must have $E_{fn}-E_{f0}\gg 0.87$ eV, which obviously is not the case.

The analysis carried out above made it clear that if the γ determined by experiments is close to unity, it cannot be interpreted as $T_c/(T+T_c)$. Thus in such a case γ does *not* reflect the *distribution* of the density of states. Since almost all amorphous silicon i-layer material used in high-efficiency solar cells has a γ close to unity, we must look into this case closely. Obviously, it must be treated with a numerical model.

III. NUMERICAL MODEL

The model is based on the physical concepts of Sec. II. However, we take into account that the density of states in amorphous silicon often has a complicated distribution, and compute the quasi-Fermi level E_{fn} numerically from Eq. (6). The energy levels in the band gap are divided into ~100 intervals with steps of 0.01 eV, then the numerical integration is carried out. Physically, this method is equivalent to using a series of discrete energy levels to replace a continuous distribution of states.[8] The number of the intervals was examined (increased to 1000) and found to have no effect on the calculated results. After the quasi-Fermi level E_{fn} is obtained from Eq. (6), the photoconductivity is calculated from Eqs. (2) and (5). Then γ is fitted with a data processing program using least-square fit.

The density of states model is composed of an exponential tail, plus deep states with a Gaussian distribution, as follows:

$$N(E)=N_0 \exp\left(-\frac{E_c-E}{kT_c}\right)+\frac{N_t}{\sqrt{2\pi}s}\exp\left(-\frac{(E-E_t)^2}{2s^2}\right). \tag{14}$$

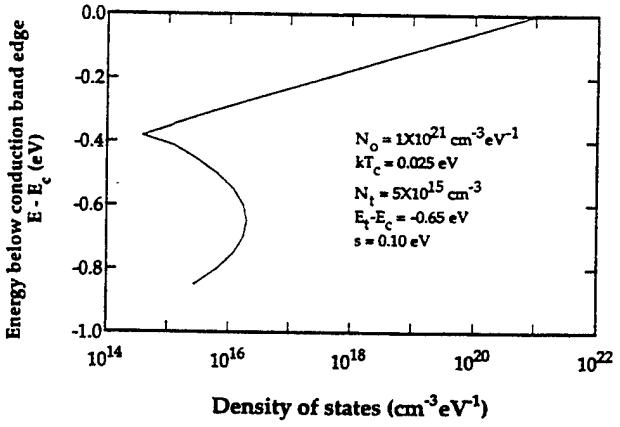

FIG. 2. Default case for the density of states $N(E)$ in the upper half of the band gap of amorphous silicon.

Here the parameters N_0, kT_c, N_t, E_t, and s are used to describe the density of states. In several calculations the Gaussian distribution was replaced by a flat distribution. Figure 2 shows a schematic plot of the density of states in the upper half of the band gap. The parameters listed in this figure are our default case. These parameters are varied systematically and the results are shown in the next section.

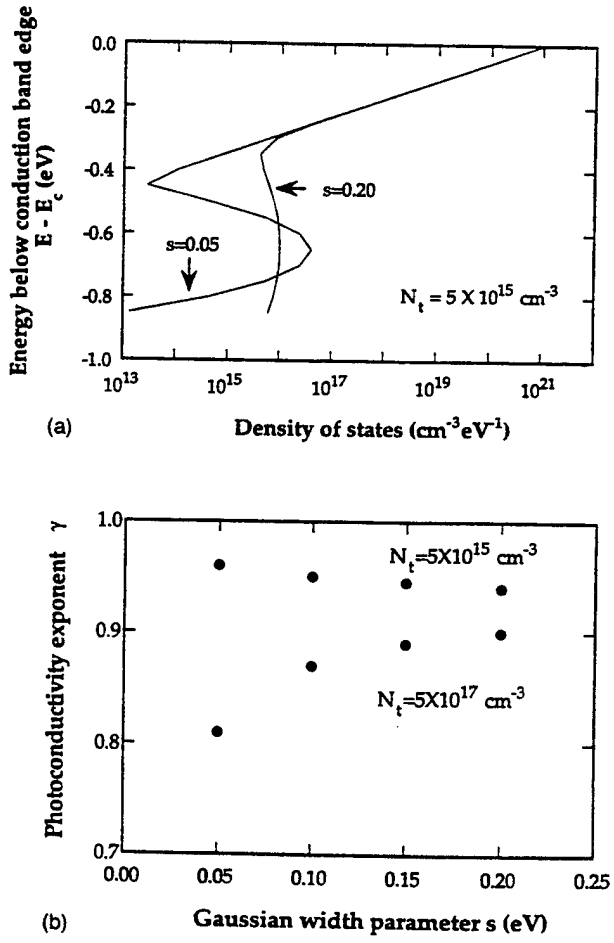

FIG. 3. (a) Density of midgap states with two different Gaussian width parameters s, but an identical total number of states N_t. (b) The photoconductivity exponent as a function of the width of the Gaussian. Note that γ remains nearly constant when N_t is low.

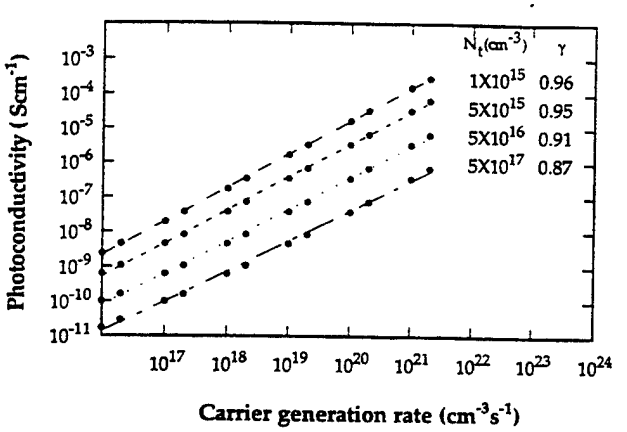

FIG. 4. The photoconductivity as a function of the carrier generation rate, for a Gaussian distribution of deep states of width $s=0.10$ eV, and total numbers N_t as shown in the figure, in cm^{-3}.

IV. RESULTS OF NUMERICAL MODELING

Since the Gaussian parameter s controls the density of states distribution, we examined the relationship between γ and s first. The total number of states under the Gaussian, N_t, was set to a constant and s was increased in steps from 0.05 to 0.10, 0.15, and 0.20 eV. Figure 3(a) illustrates the density of states for the two extreme cases of $s=0.05$ eV and $s=0.20$ eV. Figure 3(b) shows the results of the calculation, with $N_t=5\times10^{15}$ cm^{-3} for the upper curve, and $N_t=5\times10^{17}$ cm^{-3} for the lower curve.

It is clear from the figure that for a low N_t γ is *not* sensitive to the *distribution* of the density of states. Although the distribution varies drastically as s is varied [see Fig. 3(a)], γ barely changes by going from 0.96 to 0.94. On the other hand, γ decreases noticeably when the total number of states N_t increases while s is kept constant.

This result is not surprising because, according to our analysis of Sec. II, a value of γ close to unity cannot be interpreted as $T_c/(T+T_c)$, thus it should not relate to the distribution of the density of states. Only when N_t is high, γ varies with s [Fig. 3(b)], mainly because for a highly concentrated density of states (e.g., $s=0.05$ eV), part of the gap states could cease to act as recombination centers at low carrier generation rate.[9]

To clarify the relationship between γ and N_t we varied N_t from 1×10^{15} to 5×10^{17} cm^{-3}, while keeping s at 0.10 eV. The calculated γ continuously decreased from 0.96 to 0.87, as shown in Fig. 4. The photoconductivity also decreased.

A flat density of states distribution was also examined. When the density of states (DOS) was raised from 2×10^{15} to 1×10^{18} cm^{-3} eV^{-1}, γ continuously decreased from 0.94 to 0.91 (Fig. 5). Note that the DOS in Fig. 5 is the *density* of states, and thus is *not* directly comparable to N_t of Fig. 4. However, since the deep states are distributed mainly from midgap to approximately 0.35 eV below the conduction-band

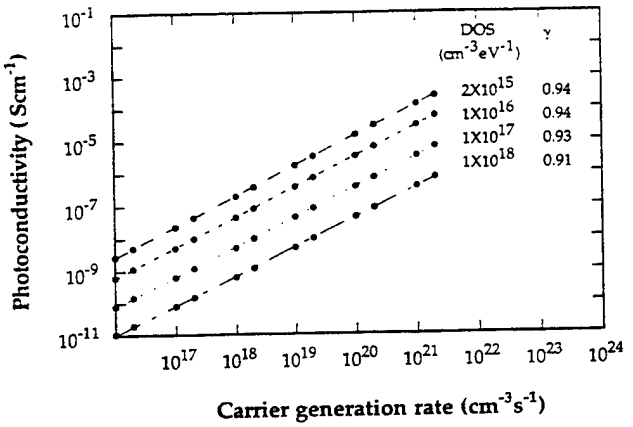

FIG. 5. Photoconductivity vs generation rate for flat distribution of deep states with densities (DOS) in $cm^{-3}\,eV^{-1}$.

edge (where the tail states become dominant), a DOS of 2×10^{15} $cm^{-3}\,eV^{-1}$ converts to a total number of deep states of roughly 1×10^{15} cm^{-3}.

To examine other factors that might affect γ, we also varied the position of the dark Fermi level E_{f0}, the density of states tail parameter kT_c and the position of the peak E_t of the Gaussian distribution. Raising or lowering the dark Fermi level E_{f0} raises or lowers the photoconductivity, but has no effect on γ. The density of tail states parameter kT_c has no effect on either photoconductivity or γ. The effect of the position of the Gaussian peak E_t on γ is more complicated, it depends on the carrier generation rate. The details will be reported elsewhere.

V. DISCUSSION

Our numerical modeling clearly shows that when γ is close to unity, it is sensitive to the total *number* of gap states rather than to their *distribution*. This is easy to understand if we examine the physics of γ closely. For an ideal photoconductive material with few recombination centers, almost all of the photogenerated carriers contribute to the photocurrent. Thus the photoconductivity will be proportional to the carrier generation rate, which means a linear relationship between σ_{ph} and G, and $\gamma\approx1$. When the number of recombination centers in the material increases, more and more photogenerated carriers are lost, thus the increase in photoconductivity lags that in the carrier generation rate, and γ becomes less than one. Thus, it is natural that γ is sensitive to the total number of midgap states.

However, a γ close to unity does not prove a low defect density. For example, if the density of states has a flat distribution, γ still can be higher than 0.9 even for a high density of states of 1×10^{18} $cm^{-3}\,eV^{-1}$. In fact, γ is set by the photoconductivity over the entire range of generation rate. Mathematically, a high photoconductivity at high generation rate together with a low photoconductivity at low generation rate leads to a high γ. Physically, the photoconductivity at high generation rate reflects the total number of states in the gap, since at high generation rate, the position of E_{fn} is high, and all gap states are included in the integral of Eq. (8). This is the reason for γ being sensitive to the total number of states in the gap. On the other hand, as discussed in preceding Sec. IV, the photoconductivity at a low generation rate is sensitive to the states near midgap. A low density of states near the midgap leads to a low γ. Thus γ alone cannot be used to conclusively determine the gap states. An alternative view on the γ was presented and discussed recently. However, we will not discuss the details in this paper. Interested readers can find the discussions in Refs. 10 and 11.

The information provided by γ is useful because it is complementary to the conductivity data. The photoconductivity measured at high generation rate is an indication of the total number of states in the gap. However, photoconductivity shifts with the dark Fermi level. Furthermore, the photo- and dark conductivities are sensitive to experimental conditions such as light intensity, electrode geometry, etc., while γ is not. Thus it is plausible to conclude that a high photoconductivity at high generation rate, a dark Fermi level close to midgap, plus a γ value close to unity suggest a low defect density in the upper half of the band gap. Combination with transient photocurrent measurements such as time-of-flight can provide an even clearer picture of density of states.[12]

Because the hole transport properties strongly affect the solar cell performance, the density of states in the lower half of the band gap is more important for these devices. The density of states in the lower half of the band gap can be measured by subgap optical absorption methods such as the constant photocurrent method or by photothermal deflection spectroscopy.[7,13,14] However, it is difficult to extract the distribution of gap states from these experiments. If the defects in the upper half and in lower half of the gap are related,[15] information about the upper half is useful for solar cells. In fact, a photoconductivity of about 5×10^{-5} S cm^{-1} at an illumination intensity of 100 mW/cm^2 of the AM 1.5 spectrum, a dark Fermi level close to midgap, plus a γ value close to unity are a quick, simple, and quite reliable rule-of-thumb for i-layer material that will produce high-efficiency amorphous silicon solar cells.[16]

The results of Sec. IV make it clear that the same γ value could correspond to many different distributions of gap states. Although a known density of states produces a certain γ, a known γ cannot be traced back to a unique density of states distribution. Thus caution should be exercised when one attempts to extract a distribution from γ.

VI. CONCLUSIONS

A numerical model was used to examine the light intensity dependence of the photoconductivity in hydrogenated amorphous silicon. The results show that the exponent γ of the photoconductivity is more sensitive to the total number of gap states rather than their distribution. A γ close to unity should be interpreted as a supplementary indication of a low total number of defect states in the material, instead of a certain distribution of these states.

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Transient photocurrent in hydrogenated amorphous silicon and implications for photodetector devices

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The transient photocurrent of amorphous silicon photodetectors is analyzed, with emphasis on its device implications. The transient photoresponse in two types of photodetector device, photoconductor and photodiode, are compared. The difference between transient photocurrent and steady-state photocurrent is discussed. Numerical modeling is used to analyze the transient photocurrent decay. The results show that response speeds in the GHz range can be achieved in amorphous silicon photodetectors with proper device structures and proper detection schemes. Potential applications are discussed. [S0021-8979(96)07102-0]

I. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) is a thin-film semiconductor developed in the 1970s. Starting with thin-film solar cells, devices based on amorphous silicon now have entered the wide field of microelectronics. Image sensors for page scanners or fax machines, thin-film transistors for liquid-crystal flat panel displays are already in commercial production. Other applications include electrophotography, particle detectors, image pickup tubes, optical recording, spatial light modulators, light-emitting devices, image sensors for high-definition television (HDTV), and two-dimensional arrays for imaging.[1–7]

The photoelectric properties of amorphous silicon have been studied by many research groups;[1–10] however, the major effort was directed toward applications with steady-state illumination or slowly varying light signals, such as in solar cells or image sensors for fax machines. While the transient photocurrent was used as a tool to explore the material properties,[11–16] few of its device implications have been discussed in detail. This article begins with a brief review of the general optoelectronic properties of amorphous silicon photodetectors, and then discusses the transient photocurrent in detail. Two types of photodetector device, the photoconductor and the photodiode, are compared. Potential device applications are discussed, with emphasis on a vertically integrated structure. In such a structure, the amorphous silicon detector arrays are integrated on top of crystalline silicon integrated circuits.

We would like to point out that the transient response of amorphous silicon under pulsed light is well known by specialists in the field. Many sophisticated experiments and models on carrier transport in amorphous silicon have been reported, and a number of devices has been demonstrated. It is not our intention to further develop the theory in this article. Our purpose is to present a concise yet complete picture of the transient phenomenon in amorphous silicon in a form that can be easily understood by many researchers in optoelectronics. A major effort was made to analyze the device implication of this transient phenomenon. Our analysis pointed out that, in contrast to the notion among many researchers who are not experts in amorphous silicon, amorphous silicon photodetector can be used in a high-speed circuit. To our knowledge, such a perspective has not been presented before. It will be our great pleasure if the gap between amorphous silicon researchers and other optoelectronic researchers can be bridged and new applications can be developed.

II. PROPERTIES OF HYDROGENATED AMORPHOUS SILICON PHOTODETECTORS

A. Steady-state illumination

Crystalline silicon is an indirect gap semiconductor. In hydrogenated amorphous silicon, however, long-range order does not exist. Because of the relaxation of the momentum-conservation rule, amorphous silicon absorbs light strongly. The optical absorption coefficient α follows Tauc's equation,[8]

$$(\alpha h\nu)^{1/2}=B(h\nu-E_g). \tag{1}$$

Here $h\nu$ is the photon energy, E_g is the optical band gap of amorphous silicon ($\approx$1.75 eV), and B is a constant. For green light with 515 nm wavelength, the α is approximately 1.4×10^5 cm^{-1}. Thus, if we use such a light source, a 100 nm thin film can absorb most of the light.

The spectral response of amorphous silicon matches visible light extremely well. Figure 1 shows a typical quantum efficiency (QE) spectrum of an amorphous silicon pin diode. The device has a structure of glass/transparent electrode/p/i/n/metal contact. We would like to emphasize that in a state-of-the-art a-Si:H p-i-n detector, the loss of photocurrent due to recombination at defect states is extremely small. The loss of QE at short wavelengths is mainly due to reflection and absorption by the glass, as well as to absorption in the transparent electrode and the heavily doped p layer. At long

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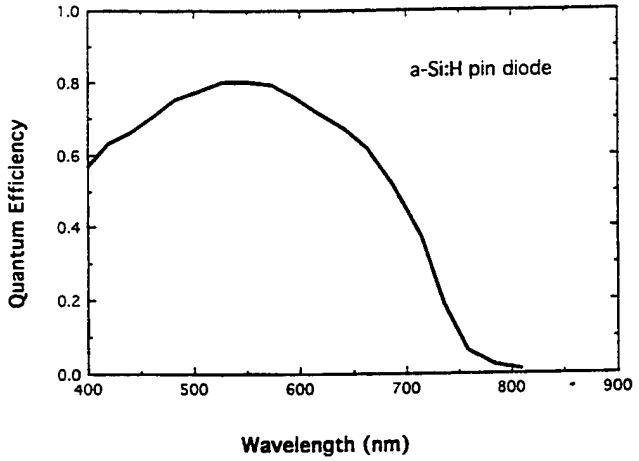

FIG. 1. A typical quantum efficiency spectrum of an amorphous silicon *p-i-n* diode.

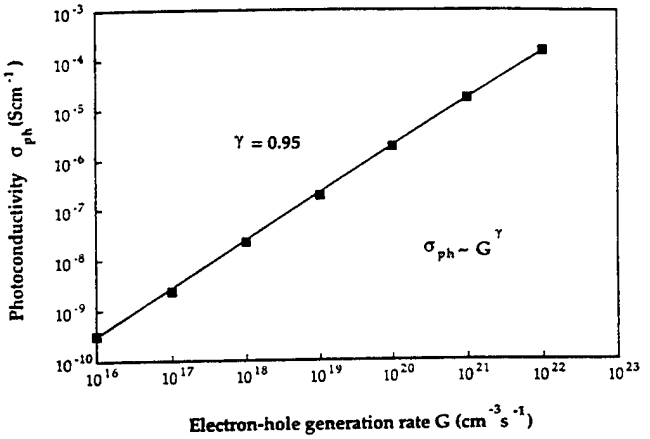

FIG. 2. Photoconductivity σ_{ph} as a function of carrier generation rate G, calculated for the density of gap states of Fig. 3.

wavelength, the QE is reduced by weak light absorption in device. By alloying with Ge, the spectral response can be extended to the near infrared.[17–21]

The steady-state photocurrent in a photoconductor is described by the photoconductivity σ_{ph}, which is dominated by the free electron density n_0 and the extended state mobility of electrons μ_0,[9]

$$\sigma_{ph}=qn_0\mu_0. \tag{2}$$

Here q is the electron charge. Since the hole mobility in amorphous silicon is much lower than that of electrons (see Sec. II D), we neglected the contribution by the hole photocurrent.

In steady state, the generation rate G of free carriers equals their recombination rate. This condition determines the free carrier density n_0,[9,22]

$$n_0=G\tau=\frac{G}{v_{th}\int_{E_{fo}}^{E_{fn}}\sigma N(E)dE}. \tag{3}$$

Here τ is electron lifetime, v_{th} is the electron thermal velocity, E_{fn} is the electron quasi-Fermi level, F_{fo} is the dark Fermi level, and σ is the capture cross section. In an amorphous semiconductor, the density of states in the energy gap often has a complicated distribution. Therefore, we prefer to compute the quasi-Fermi level numerically.[23]

The result of such a calculation is shown in Fig. 2, for the density of states shown in Fig. 3. The density of states is composed of an exponential band tail with a characteristic energy kT_c, plus a Gaussian distribution of midgap states.

From Fig. 2, it is clear that over a wide range the photoconductivity depends on carrier generation rate as

$$\sigma_{ph}=\sigma_0 G^{\gamma}. \tag{4}$$

The parameter γ is close to one when G is low. This is because the density of midgap states is low, the photoconductivity is proportional to G, thus, γ is close to one. At high G, the quasi-Fermi level enters the band-tail region.[22] The calculation is based on the assumption that all states below E_{fn} act as recombination centers. It takes into account only monomolecular recombination. The real situation at high generation rate is more complicated. We do not discuss this further here, and refer the interested reader to Ref. 9. Experimental data support the calculated results for the carrier generation rate up to $\sim 1\times10^{21}$ cm^{-3} s^{-1} (about 1 sun).[23] Few data beyond that is available because of the limitation of the light intensity; however, there is indication that Eq. (4) holds for a high light intensity.[24]

B. Amorphous silicon photodiode and photoconductive detectors

Photodetectors based on hydrogenated amorphous silicon can have a photodiode structure or a photoconductor structure. A photoconductive sensor usually has a parallel structure with two ohmic contacts defining a gap, while a photodiode sensor is a *p-i-n* diode or a Schottky diode with a vertical structure. Figure 4 shows these structures schematically.

The photodiode-type detector can be operated in a photovoltaic mode or in a reverse-biased photodiode mode. Since the response speed of the latter is much higher, we only discuss the reverse-biased amorphous silicon photodiode. This type of detector has several advantages. Since the photocurrent is only controlled by the light intensity, the de-

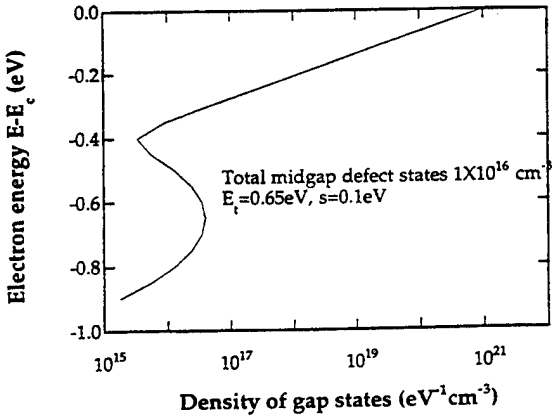

FIG. 3. A typical density of gap states in the upper half of the band gap of hydrogenated amorphous silicon.

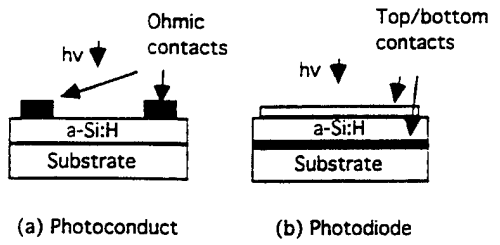

FIG. 4. Schematic structures of (a) a photoconductive-type and (b) a photodiode-type detector.

tector provides good uniformity and good control of the gray scale. A high reverse bias field reduces the transit time of the carrier, thus a short response time can be achieved. Furthermore, the reverse bias on the photodiode reduces the recombination loss; however, the photocurrent from a photodiode is usually lower than that of a photoconductive-type detector.

A photoconductive-type detector has a higher photocurrent due to the photoconductive gain. The photoconductive gain (PG) is given by[9]

$$\mathrm{PG}=\mu\tau F/L. \tag{5}$$

Here μ is the electron drift mobility,[11,12,22] F the bias electric field, and L the distance between the electrodes of the detector element.

In fact, the photoconductive gain is the ratio of electron drift length $\mu\tau F$ to the electrode spacing. The electron drift length is the distance that an electron drifts before recombination. In state-of-the-art amorphous silicon materials, the electron drift length is one to two orders longer than the typical electrode distance of a device. The electron, as a majority carrier, can "reenter" the semiconductor and further contribute to the photocurrent. If its lifetime is long, a carrier can pass through the electrodes of the external circuits several times and thus contribute to a higher photocurrent. Low-level phosphorus doping can increase the photoconductivity.[25] Thus, the steady-state photocurrent in a photoconductive-type sensor can be up to two orders higher than that of a photodiode sensor, where the reverse-biased diode structure blocks the carrier from reentering. However, as we see in the following subsection, this higher photocurrent is achieved at the expense of reduced response speed, which is not desirable for a high-speed operation.

C. Transient photocurrent in the photoconductive detector

Usually a gap structure [Fig. 4(a)] is used in this type of detector. The detector is illuminated uniformly from the top. Both electrodes make ohmic contacts and the photocurrent density j_{ph} is determined by

$$j_{\mathrm{ph}}=q\mu_0 n_0 F. \tag{6}$$

If the detector is illuminated by a light pulse, the transient photocurrent in principle still is determined by the free carrier density n_0. Only a free carrier can drift in an electrical field and contribute to the photocurrent, however, in an amorphous semiconductor, a large density of localized band tail and midgap states exists. The transport of carrier involves frequent trapping, detrapping, and motion (transport in the extended states). Thus, the free carrier density n_0 varies with time in a complicated way.

Two factors can reduce the free carrier density and cause photocurrent decay. If recombination happens, then a free carrier is lost, thus the photocurrent will be reduced; however, often the transient photocurrent starts to decay long before the recombination lifetime. Basically, this occurs because the transport of carriers in amorphous silicon involves frequent trapping and detrapping. This process leads to "deep trapping."[11,13,22] The time for which a carrier resides in a trap is determined by the energy level of the trap. Carriers which have fallen into a shallow trap are reemitted soon after capture, but carriers in a deep trap must wait longer. In principle the carrier always is reemitted if one waits long enough, but in practice beyond a certain time the transient photocurrent signal becomes too small to be distinguished from the noise. Thus, a carrier which has fallen into a deep trap effectively is lost. Since not all deep traps are recombination centers,[22] deep trapping often is the major cause for the transient photocurrent decay.

The transient photocurrent can be analyzed numerically, using a density-of-states model. The computation is simplified by replacing the continuous distribution of states with a series of discrete trapping levels $N(E_i)$.[26]

Let ω_i and γ_i be the probability of carrier capture and release at the ith trapping level, with an energy of E_i, then

$$\omega_i=N(E_i)\sigma v_{\mathrm{th}}, \tag{7}$$

$$\gamma_i=\nu_i \exp(-E_i/kT). \tag{8}$$

Here σ is the capture cross section, which we assume to be independent of E_i, and ν is the attempt-to-escape rate of the electrons. Assuming that n_0 is the density of free electrons and n_i is the density of the electrons in the ith trapping level, the kinetics of the carrier densities can be described by the following equations:

$$\begin{aligned}\frac{dn_0(t)}{dt}&=\sum_{i=1}^{m}\gamma_i n_i(t)-n_0(t)\sum_{i=1}^{m}\omega_i,\\ \frac{dn_i(t)}{dt}&=n_0(t)\omega_i-n_i(t)\gamma_i \quad (i=1,\ldots,m).\end{aligned} \tag{9}$$

Here m is the number of the energy levels. These equations can be solved numerically.[26]

Figure 5(a) shows a calculated transient photocurrent using the density-of-states model of Fig. 3. A rapid decay occurs in the short time period of picoseconds. Physically this decay corresponds to the initial thermalization of the electrons in shallow states (tail states). Since the density of tail states is high near the band gap, the trapping effect is strong and the transient photocurrent decay is very fast. After this initial decay, the photocurrent decays gradually for a time, until deep trapping causes another sharp drop. In this particular calculation, this sharp drop occurs between 10^{-8} and 10^{-7} s. To show this drop clearly, the transient photocurrent is plotted on a logarithmic scale in Fig. 5(b). Figure 5(b) also shows the calculated transient photocurrent for two other dif-

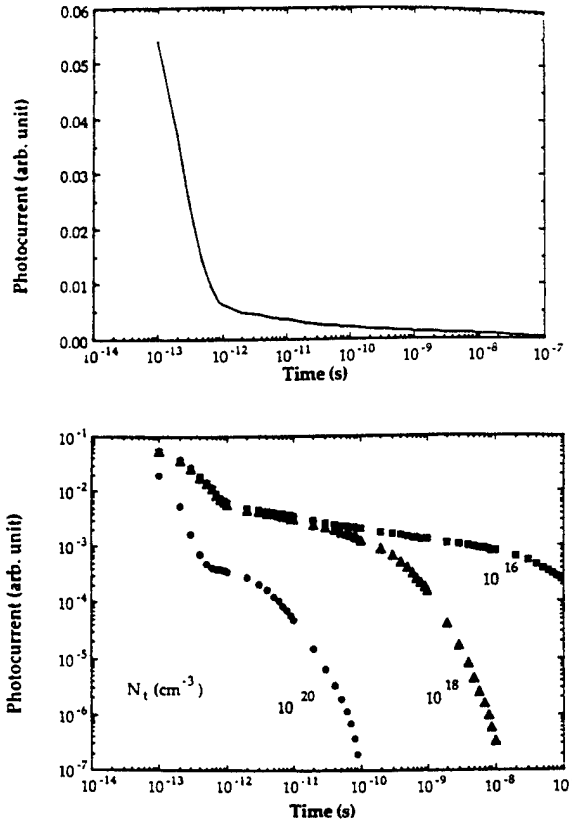

FIG. 5. (a) Calculated transient photocurrent vs time, for a midgap states N_t of 10^{16} cm^{-3}, on a linear scale. (b) The transient photocurrent for three different densities of midgap states, on a logarithmic scale.

ferent numbers of midgap states N_t. From Fig. 5(b), it is clear that the magnitude of initial photocurrent (at $t=0$) is not affected by defect density.

The calculation highlights clearly that either the initial thermalization or the deep trapping decay can be used to achieve a short response time of a device. The response time can be adjusted to between 1 and 100 ps. For a short response time, a material with high density of midgap states should be used. Actually this is a well-known method for the fabrication of high-speed switching transistors, where recombination centers are introduced intentionally to improve the response speed of the transistors.[27]

D. Transient photocurrent in the photodiode detector

In this structure, a blocking contact is used. Because the free carriers cannot reenter the device, the transient photocurrent decreases when the free carrier reaches the electrode. Thus, if the defect density is low, the transient photocurrent decay is determined by the transit time, which is the time that a carrier needs to travel through the device. Whether a transient photocurrent decay is due to transit time or lifetime can be determined through measuring the bias voltage dependence of the transient photocurrent. The transit time is voltage dependent, while the carrier lifetime is not sensitive to bias voltage.

Because of the trapping states in amorphous silicon, the transit time t_T actually includes two time components—the

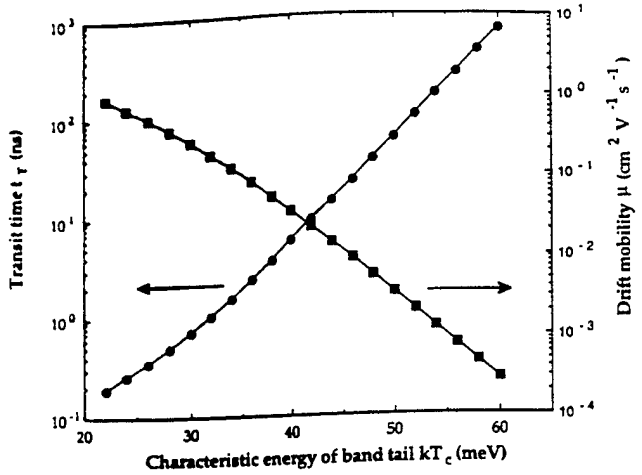

FIG. 6. Transit time t_T and drift mobility μ as functions of the band-tail characteristic energy kT_c.

time that an electron spends in the conduction band and the residence time in traps. So the transit time can be expressed as[26]

$$t_T = t_0 + \sum N(E_i)\sigma\nu_{th}t_0\nu_i^{-1}\exp\left(\frac{E_i}{kT}\right). \tag{10}$$

Here $t_0 = d/\mu_0 F$ is the time that an electron spends in conduction band. The second term is the time that an electron spends in the traps.[22] From this equation it is obvious that the transit time is shorter for a thin device under a strong bias field. Furthermore, since the density of tail states increases exponentially toward the band edge (see Fig. 3), the transit time is closely related to the characteristic energy of the band tail kT_c.[28–30]

Figure 6 shows the transit time versus kT_c, calculated using Eq. (10). The device thickness was taken as 100 nm and the bias field as 5×10^4 V/cm. The drift mobility, which is defined as $\mu = d/t_T F$, is also plotted. It is clear from the figure that for a kT_c around 27 meV, which is a typical value of the conduction-band tail, the transit time is around 0.5 ns. Thus, if the carrier lifetime is long, the transit time will determine the device response time.

One related issue here is the hole mobility. As we mentioned earlier, the hole mobility of amorphous silicon is much lower than the electron mobility. The cause is not so much a low mobility of the free hole, but a wide valence-band tail. A typical value for the characteristic energy kT_v of the valence-band tail in amorphous silicon is 50 meV. Physically, this means that a hole spends a much longer time in the traps than an electron. From Fig. 6 it is clear that if kT_c increased from 25 to 50 meV, the drift mobility would decrease by a factor of 200 and the transit time would increase correspondingly. Thus, the hole contribution to the transient photocurrent is small.

Another important feature of this type of detector is the wavelength dependence of the photocurrent, especially the mechanism of charge collection. In the following subsections we discuss the effect of wavelength briefly, and then divide our discussion in two parts according to the wavelength of light.

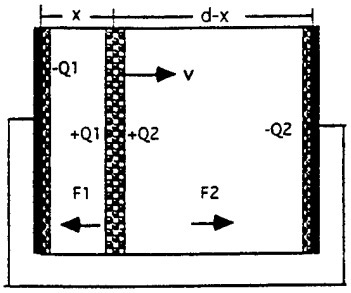

FIG. 7. Illustration of the photogenerated charge sheet, the induced field, and the charges induced on the electrodes.

If a short-wavelength light pulse is used, electron–hole pairs are generated near the front surface. Because a bias voltage is applied between the front and the back surfaces, one type of carrier will move directly into the front contact. The other type of carrier will drift across the sample. For example, if the front surface is negatively biased, then the holes will directly move into the power source, and the electrons will drift across the sample from the front to the back surface. In this case only one type of carrier will contribute to the photocurrent, and the carrier loss mechanism is deep trapping.

For long-wavelength light, electron–hole pairs are generated in the bulk. Thus, both electrons and holes contribute to the photocurrent. However, since the hole mobility in amorphous silicon is much lower than the electron mobility, the hole contribution to the photocurrent is small. The carrier loss mechanism becomes more complicated, because it involves both recombination and deep trapping; however, since the deep trapping lifetime is usually shorter than the recombination lifetime,[22] often deep trapping still is the major cause of carrier loss.

1. Short-wavelength light

Amorphous silicon is a semi-insulating material. A sheet of photogenerated carriers, drifting in an electric field, will produce a displacement current.[31,32] For the benefit of physical understanding, we concentrate our discussion on the case of sheet of charge moving inside the amorphous silicon. In a real device the sheet could be dispersive due to trapping and detrapping; furthermore, the carrier diffusion can also contribute to the photocurrent.[33]

From elementary physics, the current density j can be written as

$$j=qn(x)\mu_0 F(x)+\epsilon\frac{dF(x)}{dt}. \tag{11}$$

Here x is the position of the charge and ϵ is the permittivity of amorphous silicon. The first term, the convection current, is zero everywhere except at the position of the photogenerated charge sheet. The second term, the displacement current, is nonzero everywhere else in the sample. Figure 7 schematically shows a sheet of photogenerated carriers drifting in a sample with an average velocity of v. A dc bias is applied across the sample; however, for the transient analysis a dc source is equivalent to a short circuit.

This displacement current density j_D and collected charge Q_c was discussed by Hecht in 1932.[32] Since the original Hecht article is not easy to find, we briefly list the derivation of the equations in Appendix A. Two important conclusions can be reached from the discussion: First, the displacement current density j_D is

$$j_D=\frac{Q}{A}\frac{v}{d}. \tag{12}$$

Here Q is the charge in the drifting sheet and $v=dx/dt$ is the drift velocity of the charge sheet. A is the area and d is the distance between the electrodes. Thus, for a given device this current is controlled by the charge Q and their drift velocity. The initial photocurrent is proportional to Q_0, the photogenerated charge. When the charge carriers fell into deep traps, the charge Q in the moving sheet decreases, and the transient photocurrent is reduced.

Note that in this case recombination is not a carrier loss mechanism (only one type of carrier exists in the device). The carrier is lost through deep trapping only. In principle the carrier in the deep trap is always reemitted if one waits long enough, but in practice the actual measurement time is limited. For light pulses with high repetition rate, the charge released from the deep trap will form a tail-like base-line current. The situation is similar to that discussed in Sec. II C.

Another important point is the collected charge. The integral of the transient photocurrent gives the collected charge (see Appendix A),

$$Q_c=Q_0\frac{\mu\tau F}{d}\left[1-\exp\left(-\frac{d}{\mu\tau F}\right)\right]. \tag{13}$$

In the case where $\mu\tau F\ll d$ (defective material or long electrode distance), the collected charge is only a portion of the photogenerated charge,

$$Q_c\approx Q_0\frac{\mu\tau F}{d}. \tag{14}$$

If $\mu\tau F\gg d$, we may expand the exponential term to $1-d/\mu\tau F$, and find that $Q_c\approx Q_0$ (complete charge collection). This is easy to understand: If the drift length is much longer than the electrode spacing, obviously all generated charges will be collected.

2. Long-wavelength light

In this case both electrons and holes contribute to the photocurrent; however, since the hole mobility is low, the hole contribution to the photocurrent is small. Thus, we still concentrate our discussion on the electrons.

The electrons are distributed in depth. There are two ways to view the transient photocurrent and charge collection. In one view we can divide the distributed electrons into narrow sheets, calculate the response for each sheet, and then use superposition to find the total response. Another way to approach the transient photocurrent is to use the concept of conduction current, just like in the parallel structure, since the charge carriers fill the entire thickness of the device. We have shown in Appendix B that these two methods in fact give the same results.

The transient photocurrent density j_{ph} is the same as that in Eq. (9),

$$j_{ph}=qn_0\mu_0F.$$

The collected charge Q_c can be written as

$$\frac{Q_c}{Q_0}=\frac{\mu\tau F}{d}-\left[1-\exp\left(-\frac{d}{\mu\tau F}\right)\right]\left(\frac{\mu\tau F}{d}\right)^2. \tag{15}$$

For the case where $\mu\tau F\ll d$ we still have

$$Q_c\approx Q_0\frac{\mu\tau F}{d},$$

the same as for the case of short-wavelength light. This is easy to understand, because if the drift length is much shorter than the electrode distance, the location at which a carrier is generated is not important.

If $\mu\tau F\gg d$, we expand the exponential term to $1-d/\mu\tau F+d^2/2(\mu\tau F)^2$, and obtain $Q_c\approx\frac{1}{2}Q_0$. This result is different from the case of short-wavelength light, because if the electrons are uniformly distributed then, on average, they drift only half the distance of a sheet generated near one electrode. If we include the contribution of the holes, and if the hole drift length is also much longer than the electrode spacing, then we will have $Q_c\approx Q_0$. Even though the hole mobility is low, after integration over a long time the collected charge contributed by the hole becomes comparable to the electron contribution.

III. DEVICE IMPLICATIONS OF THE TRANSIENT PHOTOCURRENT

Now we consider the device implications of the characteristics of the transient photocurrent. Two important conclusions can be drawn from the discussion above: First, the initial transient photocurrent is determined by the density of photogenerated charge and its drift velocity, and is not controlled by the deep traps or recombination centers in the material; second, the collected charge is controlled by the deep traps and recombination centers. Conventional amorphous silicon optoelectronic devices work in a charge collection mode. To ensure complete charge collection, the defect density in the material must be low. Furthermore, if both electrons and holes need to be collected, the device response speed will be determined by the hole mobility. For example, a photovoltaic-type detector uses collected electrons and holes as signal, thus, the response speed is determined by the hole mobility.

However, to detect a transient signal, it is not necessary to insist on collecting both carriers. The nature of the displacement current suggests that electron transient photocurrent can be used as the signal. If we require complete electron charge collection, the electron transit time will determine the response time of a device.

The electron transit time is determined by the electron drift mobility, which is of the order of 1 $cm^2\,V^{-1}\,s^{-1}$ (see Fig. 6); however, when compared to a crystalline silicon photodetector, the disadvantage of low mobility is balanced by a short carrier transport path. As we mentioned, amorphous silicon has a high optical absorption coefficient. A film thinner than 0.5 μm usually is sufficient for photodetector application. This thickness is nearly two orders of magnitude lower than that of an equivalently sensitive crystalline silicon detector. If the device works in a direction perpendicular to the film surface, then the carrier transport path can be two orders of magnitude shorter in an amorphous silicon device than that in a crystalline silicon device with a similar structure. If we use a photodiode-type detector with a thickness of 100 nm, a bias field of 5×10^4 V/cm, the transit time in amorphous silicon is about 0.5 ns (Fig. 6). Thus, the device working in the electron charge collection mode could be used to detect a high-frequency signal up to 2 GHz.

Furthermore, we would like to point out that for detecting a short light pulse, it is even not necessary to insist on complete electron charge collection. Since the initial photocurrent is not affected by the deep states, a material with very short carrier lifetime can be used. The initial thermalization of the electrons into shallow traps or trapping lifetime decay can be used to form a short pulse, producing a response time shorter than the transit time. The carrier lifetime in amorphous silicon can be easily adjusted through doping, alloying or light soaking. Although little research work has been done along this line, reports do exist which suggest that this concept is feasible. For example, Smith *et al.* used highly implantation damaged silicon to study picosecond photoconductivity, and observed a response pulse of ~50 ps.[34]

One interesting issue here is the effect of the trapped charge on device performance. The trapped charge will alter the energy band bending in the device, but for a thin device with a high-bias field, this effect is minor. The trapped charge can also cause a base-line current tail, which arises from the detrapping in the long time. For single light pulse detection this is not an important issue; however, for short light pulses with high repetition rate, the modulation depth of the electric pulse will decrease.

Another related issue is the dielectric relaxation time of material and RC constant of the device. The dielectric relaxation time of amorphous silicon depends on many experimental details such as the illumination and the density of defect states in the material. Furthermore, a thin device has a higher capacitance which might lead to a high RC constant; however, in photodetector application, usually an amplifier is connected after the detector. Depending on the method of connection, the effect of the relaxation time of the material and RC constant of the device could be drastically reduced.[35] Thus, we do not discuss this issue any further.

It is also interesting to compare the transient responses of photoconductive-type to photodiode-type detectors. As we mentioned in Sec. II A, in steady-state operation the photoconductive-type detector produces a higher photocurrent; however, according to the discussion above, the situation is quite different for a transient photocurrent. The photoconductive gain is based on "recycling" the photogenerated carriers. In a high-frequency application, instead of increasing the photocurrent, a long lifetime leads to a low response speed of the device. To achieve a short response time, the detector should be designed with either a short transport path or a short lifetime.

The transient photoelectric characteristics of amorphous silicon reviewed here suggests that amorphous silicon photodetectors can be used in a high-speed system. Hydrogenated amorphous silicon can be deposited on virtually any substrate at temperatures below 200 °C by plasma-enhanced chemical-vapor deposition (CVD). Thus, it can be deposited on top of silicon integrated circuits (ICs) without damage to the circuits below. An insulator, deposited on top of the crystalline silicon chip or thin-film IC, isolates the detector elements from the circuits below. The amorphous silicon photodetector array and metal contacts can be deposited on top of the insulator. The connection between the detector and processor can be accomplished by patterning the insulator and metal using photolithographic techniques. Such a system can be used in high-speed parallel signal processing with an optical detector array vertically integrated with a processor array,[36] in optical interconnection,[37–40] or in high dynamic range wide bandwidth photodetector arrays with random access capability.[35]

IV. CONCLUSION

The transient photoelectric characteristics of amorphous silicon photodetectors were analyzed in detail. The device implications were discussed. The results show that high response speed can be achieved in amorphous silicon photodetectors with proper device structures and proper detection schemes.

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APPENDIX A

Assume that the photogenerated charge in the sheet is Q, which is distributed on the two sides of the sheet (Q_1 and Q_2). The electric fields F_1 and F_2 will be induced by the charge (see Fig. 7). According to elementary physics, the relationship is

$$-F_1x+F_2(d-x)=0, \tag{A1}$$

$$Q_1+Q_2=Q. \tag{A2}$$

Using Gauss's law, we have

$$F_1=\frac{Q_1}{A\epsilon}, \quad F_2=\frac{Q_2}{A\epsilon}. \tag{A3}$$

Here A is the area. The electric fields and charge distribution can be obtained by solving these equations,

$$F_1=\frac{Q}{A\epsilon}\left(1-\frac{x}{d}\right), \quad F_2=\frac{Q}{A\epsilon}\frac{x}{d}. \tag{A4}$$

When the charge drifts and changes its position, a displacement current j_D is induced,

$$j_D=-\epsilon\frac{\partial F_1}{\partial t}=\epsilon\frac{\partial F_2}{\partial t}. \tag{A5}$$

Substituting for F_1 or F_2 with Eq. (A4), we find

$$j_D=\frac{Q}{A}\frac{v}{d}. \tag{A6}$$

Here $v=dx/dt$ is the drift velocity of the charge.

The displacement current will induce a charge movement in the external circuit, and the charge Q_c collected in the outside circuit is determined by

$$Q_c=\int i\,dt=\int j_DA\,dt=\frac{Q\Delta x}{d}. \tag{A7}$$

Here Δx is the distance that the charge sheet drifts. From Eq. (A6), it is clear that the initial transient current is determined by the density of charge and its drift velocity, and is not controlled by the defects in the material; however, the collected charge is controlled by the distance that the photogenerated charge drifts [Eq. (A7)], and thus is controlled by the defect density. The more defects, the shorter a carrier can drift, and the less the collected charge.

It is interesting to look further into the charge collection. Because of the deep trapping, the charge Q in the drifting sheet will decrease. The loss of the free charge can be described by the electron lifetime τ,[22,27,33]

$$\frac{dQ}{dt}=-\frac{Q}{\tau}. \tag{A8}$$

After substituting $dt=dx/\mu F$ into Eq. (A8) and integrating, we have

$$Q=Q_0\exp\left(-\frac{x}{\mu\tau F}\right), \tag{A9}$$

where Q_0 is the total charge initially generated at the top surface. This equation basically tells us that the charge in the moving sheet is not a constant, but decays exponentially as the sheet moves into the device. The quantity $\mu\tau F$ is the drift length of the carrier, that is, the average distance a carrier can move before it falls into a deep trap.

Substituting Eq. (A9) into Eq. (A7) and integrating gives

$$Q_c=\int_0^d\frac{Q}{d}\,dx=\int_0^d\frac{Q_0\exp(-x/\mu\tau F)}{d}\,dx, \tag{A10}$$

and we derive the collected charge as

$$Q_c=Q_0\frac{\mu\tau F}{d}\left[1-\exp\left(-\frac{d}{\mu\tau F}\right)\right]. \tag{A11}$$

APPENDIX B

Assuming that the total photogenerated charge is Q_0 and is distributed uniformly in the device of thickness d, then the charge ΔQ in a narrow sheet Δy is $\Delta Q=Q_0\Delta y/d$ (Fig. 8). The displacement current induced by this charge sheet is $[(Q_0\Delta y/d)v]/Ad$. The total current in the external circuit is the superposition of the currents induced by all charge sheets.

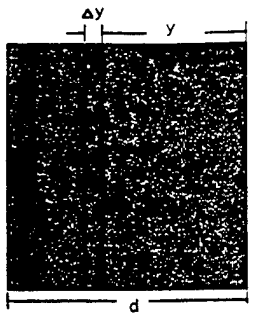

FIG. 8. In a device excited uniformly with long-wavelength light, charge transport can be analyzed via many narrow sheets.

$$j=\int_0^d \frac{(Q_0/d)v}{Ad}\,dy=\frac{Q_0 v}{Ad}. \tag{B1}$$

Since $v=\mu F$, and Q_0/Ad is the charge density qn, we find

$$j=qn\mu F. \tag{B2}$$

Because $n\mu=n_0\mu_0$,[11,12] Eq. (B2) is the same as the result obtained from a calculation of the conduction current. This is not a surprise since the definition of the displacement current guaranteed this result.

Now we consider the collected charge Q_c. A charge sheet whose distance to the electrode is y contributes to the collected charge,

$$\Delta Q_c=\left(\frac{Q_0\Delta y}{d}\right)\frac{\mu\tau F}{d}\left[1-\exp\left(-\frac{y}{\mu\tau F}\right)\right]. \tag{B3}$$

Actually this equation is the same as Eq. (A11), with y as the distance from the charge sheet to electrode, and $\Delta Q=Q_0\Delta y/d$ as the charge in the sheet.

By integrating over y we obtain

$$\frac{Q_c}{Q_0}=\frac{\mu\tau F}{d}-\left[1-\exp\left(-\frac{d}{\mu\tau F}\right)\right]\left(\frac{\mu\tau F}{d}\right)^2. \tag{B4}$$

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Carrier lifetime in amorphous semiconductors

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In amorphous semiconductors, because of the band-tail and -gap states, the excess carrier lifetime becomes sensitive to many experimental details. An attempt is made to clarify the relationship between carrier lifetime, density of states, and measurement details. The results show that in a steady-state photoconductivity measurement, the loss of carriers by recombination is determined by the density of deep states and the position of the quasi-Fermi level. In a transient measurement, the limited observation time and the contact also play important roles, besides the density of states. The shallow states in the energy band control the drift mobility and thus affect the lifetime indirectly. In an extreme case, the lifetime can become longer as the defect density increases. These points are illustrated with the electron lifetime derived from photoconductivity, time of flight, and delayed-field charge collection for hydrogenated amorphous silicon and silicon-germanium alloys.

I. INTRODUCTION

The lifetime of excess carriers is an important parameter for characterizing semiconductors; however, in amorphous semiconductors, because of the band-tail states and defect states, the carrier lifetime becomes sensitive to many details of sample preparation and of the experiments employed for the measurement of lifetime. Even for the same sample, the measured lifetime varies with measurement technique. This article attempts to clarify the relationship between carrier lifetime, energy band states, and the details of the experiment. Definitions and theories are reviewed first, then the physical origin of the differences in carrier lifetime is analyzed. Finally, we present experimental data for illustration.

II. LIFETIME OF EXCESS CARRIERS

The excess carrier lifetime in semiconductors is defined via the probability of carrier annihilation,[1]

$$\frac{dQ}{dt} = -\lambda Q. \tag{1}$$

Here Q is the excess charge carrier density and λ is the annihilation probability. The carrier lifetime τ is defined as $1/\lambda$. From a statistical point of view, τ is the average lifetime of the excess carriers.

In an amorphous semiconductor, a large density of band-tail states and midgap states exists. The transport of excess carriers involves frequent trapping, detrapping, and motion (transport in the extended states). Only free carriers—the carriers in extended states—are able to drift in an electrical field. The balance between trapping and detrapping determines the free-carrier density. The detrapping probability γ is determined by the depth of the trap energy level E and temperature T,

$$\gamma = \nu_0 \exp(-E/kT). \tag{2}$$

Here the ν_0 is the attempt-to-escape frequency and k is the Boltzmann constant. The energy level E is referenced to the boundary between extended states and localized states—the conduction-band edge for electrons and the valence-band edge for holes. The reciprocal of γ is the carrier residence time t_{res} in the trap,

$$t_{res} = \nu_0^{-1} \exp(E/kT). \tag{3}$$

A carrier which falls into a shallow trap can be reemitted into the extended states within a short time and then becomes mobile again. Actually, this is the definition of a shallow trap. It takes a long time for a carrier in a deep trap to be reemitted, and frequently recombination takes place during this time.[2] Thus, only deep traps affect the recombination lifetime of a carrier. We point out later that the division between the "shallow" and "deep" trap depends on experimental details; However, for convenience we call the states which directly control the carrier lifetime the "deep states."

In a crystalline semiconductor, the carrier lifetime τ is related to the density of recombination center states N_t as follows:[1]

$$\tau = 1/(v_{th}\sigma N_t). \tag{4}$$

Here v_{th} is the thermal velocity of the carrier. v_{th} is a good approximation to the carrier velocity in an electric field, because usually the drift velocity of the carrier is much lower

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than the thermal velocity, if the electric field is not too strong. σ is the capture cross section. The term $v_{\rm th}\sigma N_t$ is the capture probability.

In an amorphous semiconductor, it appears that if we replace N_t by an integral over the density of deep states, the lifetime should follow the same equation; however, if we look into the physics of the equation, this "lifetime" actually corresponds to a probability of a free carrier being captured by a deep state, since a carrier which is trapped in shallow states is not mobile and thus will not be able to "meet" the deep traps. We label this lifetime as τ_f,

$$\tau_f=\left(v_{\rm th}\int \sigma N(E)dE\right)^{-1}. \tag{5}$$

$N(E)$ is the density of deep states ($\rm cm^{-3}\,eV^{-1}$). As we mentioned, the transport of a carrier in an amorphous semiconductor is a process that involves frequent trapping and detrapping from the shallow states, and motion. The average carrier lifetime τ includes two components. One is the time that the carrier spends in the extended states. In fact, this is the free-carrier lifetime τ_f, since the average travel distance is $\tau_f v_{\rm th}$, and the velocity of the carrier is close to $v_{\rm th}$. The second, and predominant, part is the residence time during which the carrier resides in the shallow traps. This residence time can be written as the summation of the residence time of a given carrier in various shallow trap levels. In case of a continuous distribution of trap states, the summation can be replaced by an integral. The number of the trap levels between E and $E+dE$ is $N(E)dE$. Actually, a trap level could trap a carrier several times during its lifetime. So, the residence time in trap levels between E and $E+dE$ is the product of the number of capture events, $\sigma v_{\rm th}\tau_f N(E)dE$, and the residence time in the trap, $\nu_0^{-1}\exp(E/kT)$. Thus, the average carrier lifetime is

$$\tau=\tau_f+\int \sigma v_{\rm th}\tau_f\nu_0^{-1}\exp\left(\frac{E}{kT}\right)N(E)dE \tag{6}$$

or

$$\tau=\tau_f\left[1+\int \sigma v_{\rm th}\nu_0^{-1}\exp\left(\frac{E}{kT}\right)N(E)dE\right]. \tag{7}$$

Now we show that the term

$$1+\int \sigma v_{\rm th}\nu_0^{-1}\exp\left(\frac{E}{kT}\right)N(E)dE$$

actually is the ratio of the drift mobility μ_d to the extended states mobility μ_0.

By definition, the drift mobility μ_d is[2]

$$\mu_d=d/(Ft_T). \tag{8}$$

Here d is the sample thickness, F is the strength of the electric field, and t_T is the transit time. Similar to the lifetime, the transit time also includes two time components: the time that the carrier spends in extended states and the residence time in traps. So the transit time can be expressed with an equation similar to Eq. (6), with τ replaced by t_T, and τ_f replaced by $d/\mu_0 F$. The term $d/\mu_0 F$ is the time that the carrier spends in extended states, before it drifts out of the sample. We have

$$t_T=\left(\frac{d}{\mu_0 F}\right)\left[1+\int \sigma v_{\rm th}\nu_0^{-1}\exp\left(\frac{E}{kT}\right)N(E)dE\right]. \tag{9}$$

Solving for t_T from Eq. (8) and substituting it into Eq. (9), one obtains

$$\left[1+\int \sigma v_{\rm th}\nu_0^{-1}\exp\left(\frac{E}{kT}\right)N(E)dE\right]=\frac{\mu_0}{\mu_d}. \tag{10}$$

Using Eqs. (5), (7), and (10), we find the relationship between excess carrier lifetime and the density of deep states in an amorphous semiconductor,

$$\tau=\tau_f\left(\frac{\mu_0}{\mu_d}\right)=\mu_0\left(\mu_d v_{\rm th}\int \sigma N(E)dE\right)^{-1}. \tag{11}$$

From this equation, it is clear that the lifetime is related to the density of defects, since defects usually introduce deep states. This is a well-known conclusion. The points we would like to emphasize here are: first, the boundary of the integral in Eq. (11) is controlled by many details such as the quasi-Fermi level, which is related to the density of deep states and the excitation rate. Second, although the shallow states do not control the lifetime τ directly, they do control the drift mobility μ_d and thus affect τ indirectly. In an extreme case, if a material is made to have more deep states but a lower drift mobility, the lifetime could become longer. The last point is that the lifetime is controlled by many experimental details. Therefore, it is not a well-defined quantity in amorphous semiconductors, and we think that is the reason behind many contradictions between experimental data. In the following sections, we analyze some examples in detail.

III. LIFETIME DERIVED FROM PHOTOCONDUCTIVITY MEASUREMENT

The photoconductivity $\sigma_{\rm ph}$ is determined by the free electron density n and the extended state mobility μ_0,[2]

$$\sigma_{\rm ph}=nq\mu_0. \tag{12}$$

Here q is the electron charge. For simplicity, we do not include the contribution of the hole current.

In steady state, the free-carrier generation rate G equals the recombination rate. This condition determines the free-carrier density,

$$n=G\tau_f. \tag{13}$$

Note that τ_f is the lifetime of a free electron. The average recombination lifetime can be easily derived from Eqs. (11), (12), and (13),

$$\tau=\tau_f(\mu_0/\mu_d)=\sigma_{\rm ph}/(q\mu_d G). \tag{14}$$

Equation (14) clearly shows that the recombination lifetime is related to the generation rate G (light intensity). Furthermore, since $\sigma_{\rm ph}$ is also related to the light intensity, the actual relationship is complicated. This relationship can be clarified by considering the quasi-Fermi level.

Under illumination, the quasi-Fermi levels split. The states between the dark Fermi level E_{f_0} and the quasi-Fermi levels are occupied and become recombination centers.[2] The

carrier loss mechanism is the recombination. Thus, the lifetime τ_{ph} derived from the photoconductivity can be written as

$$\tau_{ph}=\left(\frac{\mu_0}{\mu_d}\right)\tau_f=\mu_0\left(\mu_d v_{th}\int_{E_{f_0}}^{E_{f_n}}\sigma N(E)dE\right)^{-1}. \quad (15)$$

E_{f_n} is the quasi-Fermi level for electrons. In an amorphous semiconductor, the density of states often has a complicated distribution. Therefore, it is preferable to compute the quasi-Fermi level numerically.

By definition, the quasi-Fermi level is used to describe the free-carrier density,

$$n=N_c\exp[-(E_c-E_{f_n})/kT]. \quad (16)$$

Here N_c is the effective density of states in the conduction band, and E_c is the energy of the conduction-band edge.

Using Eqs. (13), (15), and (16), we obtain

$$N_c\exp\left(-\frac{(E_c-E_{f_n})}{kT}\right)=G\left(v_{th}\int_{E_{f_0}}^{E_{f_n}}\sigma N(E)dE\right)^{-1}. \quad (17)$$

For a given carrier generation rate G and a density of gap states distribution $N(E)$, the quasi-Fermi level E_{f_n} can be computed from Eq. (17) numerically.

Since τ_{ph} is determined by the total number of states below E_{f_n}, details of the distribution of the states below E_{f_n} have little effect on the photoconductivity. However, if we disturb the system by, say, shifting the dark Fermi level E_{f_0} through intentional or unintentional low-level doping, or by generating deep states through light soaking, then the responses of such materials with different distributions of states could become different from each other. In a system with a Gaussian-like distribution of states, the Fermi level could shift rapidly at low G and then become pinned at the Gaussian peak. Thus, if the defect density is low, the photoconductivity may be drastically changed by low level doping.[3] On the other hand, if the defect density is high, the Fermi level E_{f_n} lies deep in the gap, and part of the defect states could come to lie above E_{f_n} and cease to act as recombination centers. Thus, the distribution of the defect states may affect the carrier lifetime.

Figure 1 shows the results of a calculation of the recombination lifetime versus the total density of midgap defect states, using Eqs. (17), (12), and (14). Three density-of-states models are used. All three models use the same conduction-band-tail-state distribution and the same total number of midgap states but with different distributions. The carrier generation rate is taken to be the high value of 10^{21} $cm^{-3}\,s^{-1}$. In Fig. 1, the triangles correspond to a distribution of the midgap states that is flat between 0.35 eV below E_c, and E_{f_0}. The round dots and square dots correspond to Gaussian-like deep-state distributions. The energy position of the Gaussian peak E_t and the width of the Gaussian s are indicated in the figure. Here E_t (eV) is reference to (below) the conduction-band edge. An arbitrary unit is used for the lifetime to avoid the complications such as setting the value of μ_0. This unit is the same for all three distributions. A

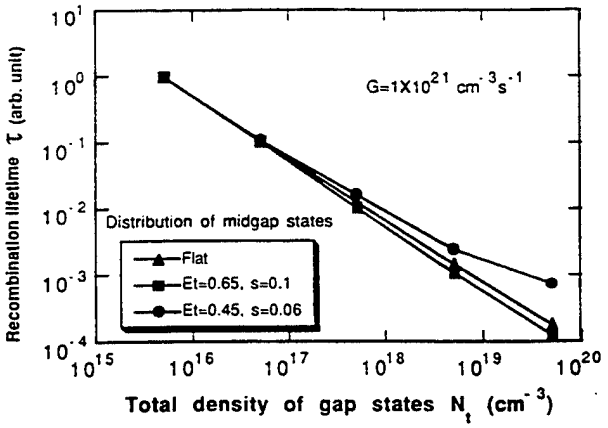

FIG. 1. Calculated recombination lifetime vs the total density of midgap states. The carrier generation rate G is 10^{21} $(cm^{-3}\,s^{-1})$.

density-of-states diagram of the upper half of the band gap and deep states with a Gaussian distribution centered at E_t=0.65 EV below E_c are shown in Fig. 2.

It is interesting to note that in the case of a high-deep-level density of states (round dots), a small down-shift of the Fermi level (toward midgap) will put a large number of states above it. These states then will cease to act as recombination centers. In this case, the lifetime decay versus the total density of midgap state becomes slower.

Another interesting point is that when the defect state is low, the detailed density-of-states distribution has little effect on the lifetime. All three curves of Fig. 1 converge to the same lifetime. The reason is that when the number of midgap states is low, the position of the quasi-Fermi level is high (close to conduction-band edge). Then all defect states act as recombination centers.

However, if we reduce the carrier generation rate, the result can become quite different. Figure 3 shows the recombination lifetime at a carrier generation rate of 10^{18} $cm^{-3}\,s^{-1}$, with all other conditions being the same as in Fig. 1. Since, under low excitation, the quasi-Fermi level lies close to midgap, the distribution of the midgap states has a strong effect on the lifetime, even when their density is low.

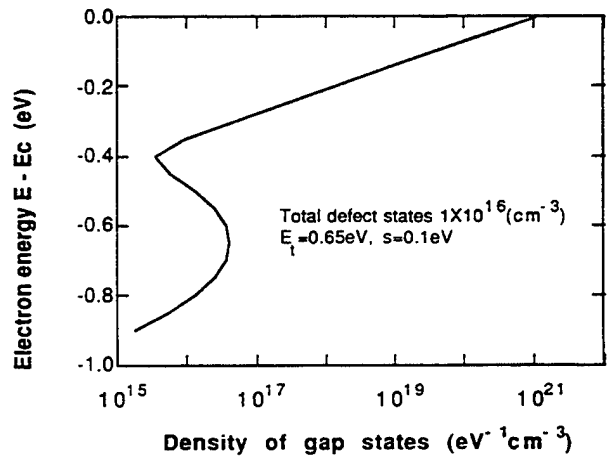

FIG. 2. Density of states diagram of the upper half of the band gap.

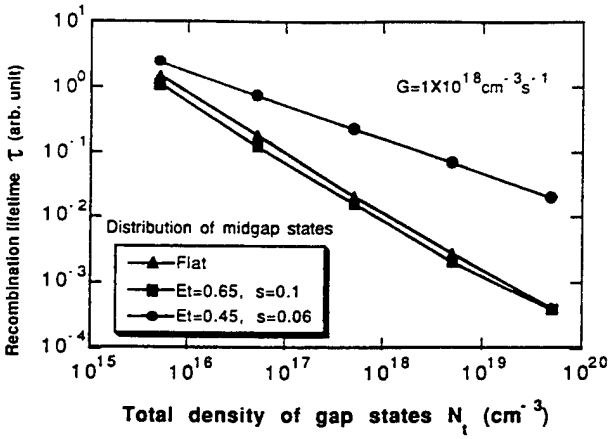

FIG. 3. Same as Fig. 1 but the carrier generation rate G is reduced to 10^{18} ($cm^{-3}\,s^{-1}$). Note the difference in lifetime.

The most prominent consequence in Fig. 3, for the Gaussian distribution with $E_t=0.45$ eV and $s=0.06$ eV, is the much smaller drop in lifetime with the increasing density of defect states.

Figure 4 shows the recombination lifetime versus the carrier generation rate for the Gaussian-like density-of-states model with $E_t=0.45$ eV and $s=0.06$ eV. The total density of midgap states is indicated in the figure. From Fig. 4 it is obvious that the lifetime is not just determined by the density of defects, but that it is also a function of the carrier generation rate.

IV. LIFETIME DERIVED FROM TIME-OF-FLIGHT EXPERIMENTS

In a time-of-flight (TOF)[4,5] experiment, electron-hole pairs are generated near the front surface of the sample by a short-wavelength, strongly absorbed, laser pulse. A voltage is applied between the front and the back surfaces, so that one type of carrier will move directly into the front contact. The other type of carrier will drift across the sample. For example, if the front surface is negatively biased, then the holes will move into the power source directly, and the electrons will drift across the sample from the front to the back surface. Because of this geometry structure, the situation is different from the TOF experiments in crystalline materials, where both carriers might exist in the sample.

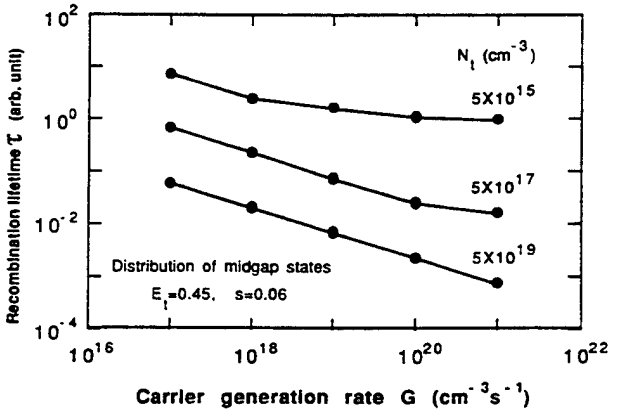

FIG. 4. Calculated recombination lifetime vs carrier generation rate. The total density of midgap states N_t is indicated in the figure.

The moving carrier will generate a transient photocurrent, which is measured as a displacement current.[6] The integral of the transient photocurrent as a function of time is the collected charge. Since only one type of carrier exists inside the sample, recombination can only happen near the surface. In the bulk, recombination is not a major loss mechanism. Many groups have noted that the lifetimes derived from steady-state and transient experiments are different. This difference is partially explained by the different carrier loss mechanisms in steady-state and transient experiments.[7–11]

Transport in TOF still involves trapping, detrapping and motion of the carriers. The time for which a carrier resides in a trap is determined by Eq. (3). Carriers in a shallow trap are reemitted soon after capture, but carriers in a deep trap have to wait longer. Within time t, all carriers in traps with an energy shallower than $E=kT\ln(\nu_0 t)$ are reemitted, while those trapped in states deeper than this energy are not. In principle the carrier always is reemitted if one waits long enough, but in practice the actual measurement time is limited. Beyond a certain time $t_{\max}$ the transient photocurrent signal becomes too small to be distinguished from the noise. Thus, a demarcation energy level E_d, determined by the maximum measurement time $t_{\max}$, can be used to distinguish the "shallow" from "deep" levels,

$$E_d=kT\ln(\nu_0 t_{\max}). \tag{18}$$

All the carriers that become trapped in an energy level below E_d can be considered lost. This is the major carrier loss mechanism in the TOF experiment—deep trapping. Equation (18) shows that E_d is sensitive to the measurement temperature. The possibility of using the temperature-dependent TOF mobility-lifetime product to explore the distribution of deep states was reported previously.[5]

Using an argument similar to the one used in the case of steady-state photoconductivity, the probability for capture of a free electron by a deep trap is

$$v_{\rm th}\int_{E_{f_0}}^{E_d}\sigma N(E)dE. \tag{19}$$

The carrier lifetime determined by TOF is

$$\tau_{\rm TOF}=\mu_0\left(\mu_d v_{\rm th}\int_{E_{f_0}}^{E_d}\sigma N(E)dE\right)^{-1}. \tag{20}$$

This equation is essentially the same as Eq. (15), with E_{f_n} replaced by E_d. Since the E_d here and the quasi-Fermi level E_{f_n} in photoconductivity are not directly related, it is not surprising that the lifetimes derived from these two experiments are different, even if the sample (and the density of deep states) is the same.

Figure 5 shows the calculated ratio of the recombination lifetime $\tau_{\rm ph}$ to $\tau_{\rm TOF}$. The carrier generation rate G in photoconductivity is taken to be 10^{21} $cm^{-3}\,s^{-1}$. The three density-of-states models are the same as the ones used for Figs. 1 and 3. $\tau_{\rm TOF}$ is calculated from Eq. (20), with E_d set at 0.4 eV.

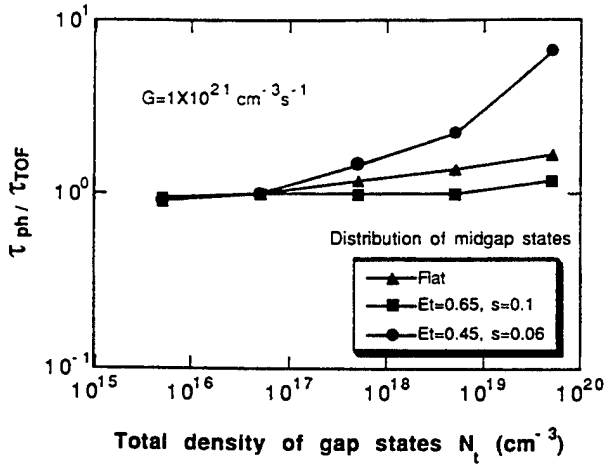

FIG. 5. Calculated ratio of the photoconductivity lifetime τ_{ph} to time-of-flight lifetime τ_{TOF} for a carrier generation rate of 10^{21} $cm^{-3}s^{-1}$. The density-of-states models are the same as the ones used for Figs. 1 and 3.

Since the observation time in TOF is ~10 μs, E_d should be ~0.4 eV (if $\nu_0 \sim 10^{12}$ s^{-1}). The τ_{ph}/τ_{TOF} ratio becomes larger when the defect density increases. This is because of the short time window, where almost all defect states act as deep states in TOF, but in photoconductivity raising the defect density lowers the quasi-Fermi level, so that the high-lying defect states cease to act as recombination centers. As a result, the difference between the lifetime in two cases increases as the defect density is raised.

All curves in Fig. 5 appear to converge to a lifetime ratio of one when the defect density is low; however, this appearance is peculiar to our assumptions. The curves converge simply because at the assumed generation rate G (10^{21} cm^{-3} s^{-1}) and number of defect states, the quasi-Fermi level E_{f_n} in photoconductivity happens to lie close to E_d in TOF.

When other values are assumed for the carrier generation rate G, the curves separate. Figure 6 shows the result of a calculation that uses a carrier generation rate G of 10^{18} cm^{-3} s^{-1}. All other conditions are the same as that used for Fig. 5. It is clear that when the generation rate in photoconductivity is reduced, the quasi-Fermi level drops. On the other hand, τ_{TOF} does not change with G. Thus, the ratio of lifetime increases.

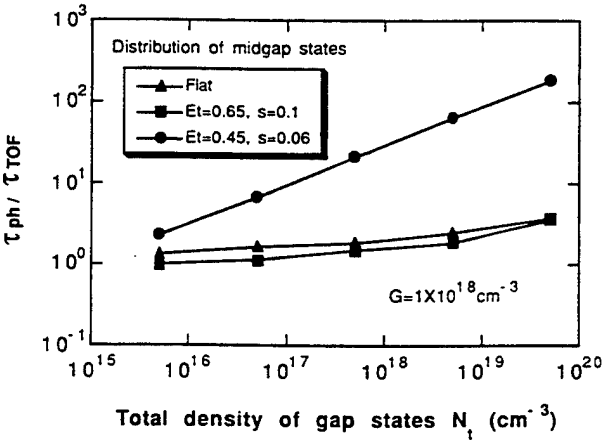

FIG. 6. Same as Fig. 5 but for a carrier generation rate of 10^{18} cm^{-3} s^{-1}.

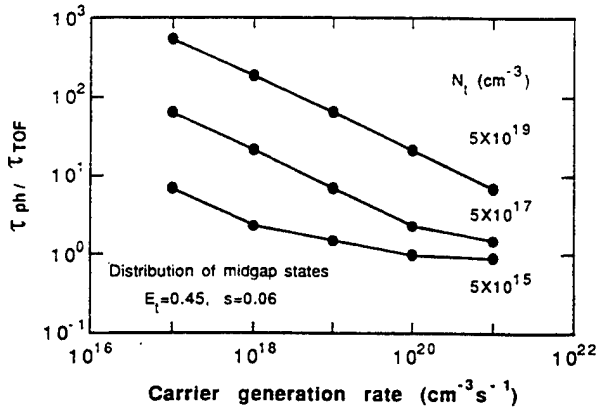

FIG. 7. Calculated τ_{ph}/τ_{TOF} vs carrier generation rate. The density-of-states model is the same as the one used for Fig. 4.

Figure 7 shows the calculated τ_{ph}/τ_{TOF} ratio versus G. The density-of-states model is the same as the one used for Fig. 4. It is clear that τ_{ph} can be two orders of magnitude longer than τ_{TOF}, if the carrier generation rate in photoconductivity is low and the defect density is high.

In practice, the TOF lifetime is derived from the dependence of the collected charge Q on the bias field F, according to the Hecht equation[6–9]

$$Q/Q_0=(\mu_d\tau_{TOF}F/d)[1-\exp(-d/\mu_d\tau_{TOF}F)]. \quad (21)$$

Here Q is calculated from the time integral of the transient photocurrent. Q_0 is the total photogenerated charge, and d is the sample thickness. A fit of Q/Q_0 to F according to Eq. (21) gives the $\mu_d\tau_{TOF}$. The drift mobility μ_d can be directly determined from the transit time in the TOF experiment, and the lifetime is obtained from $\mu_d\tau_{TOF}$ and μ_d.

The Hecht equation is derived from the displacement current induced in the electrodes by a moving charge, and the carrier lifetime defined by Eq. (1). The derivation of this equation assumes a uniform and constant electric field F. To insure that this is the case in a given experiment, a low light intensity must be used, so that the field induced by the photogenerated charge is negligible compared to the field set up by the external bias. Thus, the electron quasi-Fermi level in this experiment lies close to the dark Fermi level E_{f_0}. This is one of the differences between the time-of-flight experiment and the delayed-field charge collection experiment described in the following section.

V. LIFETIME DERIVED FROM DELAYED-FIELD CHARGE COLLECTION

The delayed-field charge collection (DF) experiment[12,13] provides an independent means to measure the excess carrier lifetime. Both the photoconductivity and TOF rely on a measurement of the mobility, while delayed-field experiment does not.

In the DF experiment a long-wavelength laser pulse uniformly generates electron-hole pairs in the sample. After a delay time t_{delay}, an electric-field pulse is applied to the

sample to collect all remaining excess carriers. During the waiting period t_{delay}, the density of excess carrier will decrease because of recombination. Using the definition of the recombination lifetime τ, we solve Eq. (1) to obtain

$$Q = Q_0 \exp(-t_{delay}/\tau). \tag{22}$$

A fit of the Q/Q_0 data to the delay time t_{delay} produces the lifetime τ.

In practice, the electrical sweep-out pulse itself generates a transient current, since the sample resembles a RC circuit. To determine this contribution to the sweep-out currents, the remaining excess carrier charge is derived from the difference between the transient currents with and without illumination. This correction can be accomplished through hardware or software.

Unlike in TOF, both electrons and holes exist inside the sample in the DF experiment. Therefore, both recombination and deep trapping can contribute to the loss of carrier. In fact, these two processes coexist. During the waiting period and the sweep-out, carriers are lost through recombination and are further reduced by deep trapping. One might think that the lifetime derived from the delayed-field experiment is shorter than that derived from TOF; however, often this is not the case.

First, this experiment is not restricted by the low-light-intensity condition of TOF (see last paragraph of Sec. IV). Since the excess carrier charge is derived from the difference between the electrical field with and without light, a strong light often is used to reduce the error. While a strong light produces a higher quasi-Fermi level, it enables a much longer observation time in the experiment. According to our preceding discussion, a longer observation time implies that fewer states will act as deep traps. Furthermore, since the light absorption is not restricted to the surface layer, the effect of surface states is reduced. (The effect of surface states is discussed in the following section). The generation rate at the surface can be made lower than that in TOF even if the total absorbed light intensity is higher. Thus, in delayed-field experiments one often observes a longer lifetime than the lifetime derived from TOF.

VI. CONTACTS AND SURFACE STATES

The difference between the lifetimes is also related to other experimental conditions, such as the contact and surface states.

Blocking or ohmic contacts have different effects on the measured carrier lifetime. Usually the photoconductivity measurement is carried out with a coplanar structure, but TOF and delayed-field experiments use vertical structures. The vertical structure uses a blocking contact (in a reverse-biased p-i-n diode or a Schottky barrier) and measures a primary photocurrent.[2] Because of the blocking contact, a carrier cannot reenter the sample. Photoconductivity in a coplanar structure uses ohmic contacts and measures a secondary photocurrent. If the recombination lifetime is long, the carrier can reenter the sample and further contribute to the photocurrent. The ratio of the secondary photoconductivity to the primary photoconductivity is the well-known photoconductivity gain. In device-quality amorphous semiconductors the recombination lifetime usually is longer than the transit time. Thus, the lifetime measured by photoconductivity often is longer than the one measured by TOF, since the latter is limited by the transit time.

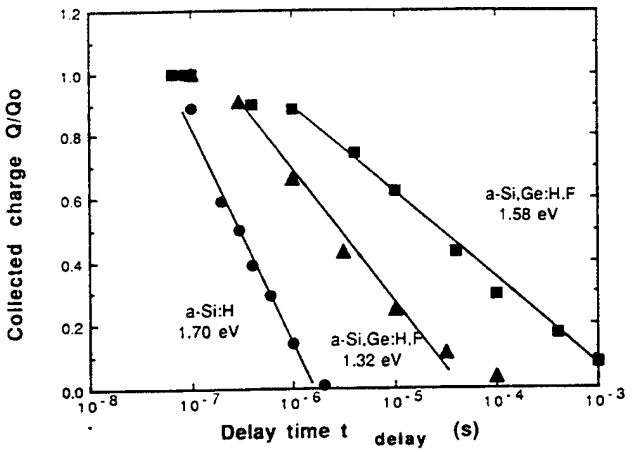

FIG. 8. Delayed-field charge collection data for three samples.

The transient $\mu\tau$ recently was measured on a coplanar structure.[14] Since the transport path becomes much longer than in a vertical structure, the observation time for the photocurrent can be longer, given a strong light excitation pulse. As a result, emission of carriers from deep states was observed. This experiment showed that recombination takes place after a multistep process of deep trapping and thermal emission. Thus, we expect a longer lifetime from photoconductivity than from TOF.

In the delayed-field experiment, the delay time (waiting period) can be much longer than the transit time. Thus, the effect of transit time on the experimental result is small. However, the DF experiment measures the primary photocurrent, and the excitation is pulsed instead of cw light, so the DF lifetime can still be significantly different from the photoconductivity lifetime.

Surface states have a strong effect on the TOF experiment since most of the light is absorbed close to the surface. The effect of surface states is most obvious in some samples with high-surface-state density.[15] Because the delayed-field experiment uses long-wavelength light, it is less affected by surface states.

VII. COMPARISON OF CARRIER LIFETIMES IN SPECIFIC SAMPLES

To illustrate the preceding discussion, we now compare the lifetimes determined by the photoconductivity, time-of-flight, and delayed-field charge collection techniques in three samples.

Figure 8 shows data from delayed-field charge collection in an a-Si:H sample and two a-SiGe:H,F alloys. The lifetimes can be derived from a fit of Eq. (22) to the linear portion of the data. The fits are shown in the figure.

All three samples were deposited by plasma-enhanced chemical-vapor deposition. The samples used in the TOF and delayed-field experiments have vertical structures, with Pd Schottky diodes on the front surfaces and Cr contact on the

TABLE I. Electron lifetime derived from photoconductivity τ_{ph}, TOF (τ_{TOF}), and delayed-field charge collection τ_{DF}.

Sample	Material	E_c (eV)	τ_{ph} (s)	τ_{TOF} (s)	τ_{DF} (s)
A	*a*-Si:H	1.70	1.6×10^{-6}	2.8×10^{-8}	5.0×10^{-7}
B	*a*-Si.Ge:H.F	1.58	6.0×10^{-5}	2.0×10^{-7}	4.5×10^{-4}
C	*a*-Si.Ge:H.F	1.32	3.0×10^{-5}	6.5×10^{-7}	8.3×10^{-6}

back surfaces. The samples used in the photoconductivity measurements have coplanar structures, with Cr parallel line patterns evaporated on the top surfaces. The *a*-SiGe:H.F samples have higher defect densities[16] and lower electron mobilities[17,18] than *a*-Si:H. The electron drift mobility becomes lower due to a widening of the conduction-band tail with Ge alloying. For example, the electron drift mobility in the *a*-Si:H sample A is 0.8 $cm^2\,V^{-1}\,s^{-1}$. In alloy sample B the electron drift mobility is reduced to 0.04 $cm^2\,V^{-1}\,s^{-1}$. In the low-gap alloy sample C deep trapping occurs before the transit time at room temperature. Therefore, the transit time can be measured only at elevated temperature (50–100 °C) and then be extrapolated to room temperature. The details of transient carrier transport in these materials are discussed in Ref. 9, and the surface states are discussed in Ref. 15. We think the change of optoelectronic properties in the alloys are related to alloy effects and deposition details. The variation of band gap itself should not introduce such changes in properties.

Table I lists the electron lifetimes derived from photoconductivity, time of flight and delayed field. The carrier generation rate in the photoconductivity measurement was $\sim10^{21}$ $cm^{-3}\,s^{-1}$, in TOF the total generated charge was $\sim10^{-10}$ C, and total charge generated in DF was $\sim10^{-9}$ C.

In all three samples τ_{TOF} has the lowest value. This is easy to understand according to the preceding discussion, because TOF uses a low light intensity and a vertical sample structure. The delayed-field experiment gives a longer lifetime than TOF, probably because of the higher light intensity used in the experiment, which enables a longer observation time. The photoconductivity in general (but not always) exhibits an even longer lifetime, which we think that is a consequence of the different carrier loss mechanism and the coplanar sample structure.

The most surprising result here is that all three lifetimes in sample C are higher than in sample A, although CPM data[16] confirm that the defect density in sample C is the highest. The most important confirmation of this fact is provided by the delayed-field data, because this technique does not rely on the measurement of mobility, which is not a well-defined quantity in a defective material.

How can the lifetime become longer while the defect density increases? The answer, although not obvious at first, is actually quite simple: In transport via multiple trapping and detrapping, carriers move in extended states; they fall into and jump out of shallow traps. If a carrier hits a deep state, it is lost. The lifetime is actually the ratio of the mean travel distance to the mean velocity. The travel distance is determined by the deep-level density. The more deep levels, the shorter the distance. The mean velocity is controlled by the drift mobility. In *a*-Si.Ge alloys, the drift mobility is much lower than that in *a*-Si:H.[17,18] Since the mobility drops faster than the defect density rises, the lifetime becomes longer. Equations (15) and (20) are merely mathematical descriptions of this physical phenomenon.

VIII. CONCLUSION

The lifetime of excess carrier in amorphous semiconductors was discussed in detail. The results show that the lifetimes in steady-state and transient experiments are controlled by different loss mechanisms. Both shallow states and deep states affect the lifetime. The lifetime is also related to many experimental details such as the light intensity, the position of the quasi-Fermi level, the surface state density, and the contacts to the sample. Thus, the lifetime in an amorphous semiconductor is not a well-defined quantity, and care has to be taken in interpreting and comparing results from different experiments.

ACKNOWLEDGMENTS

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